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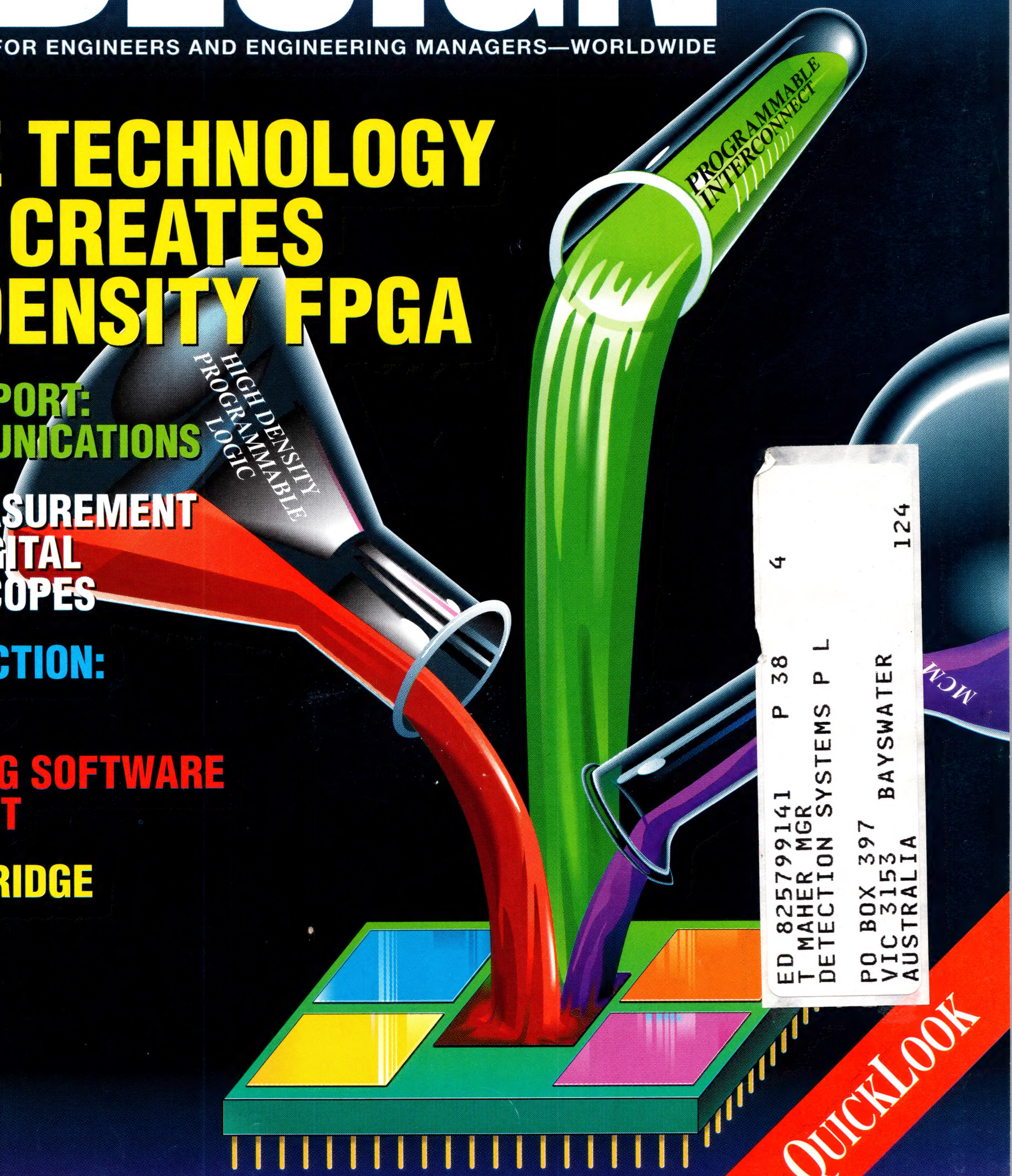

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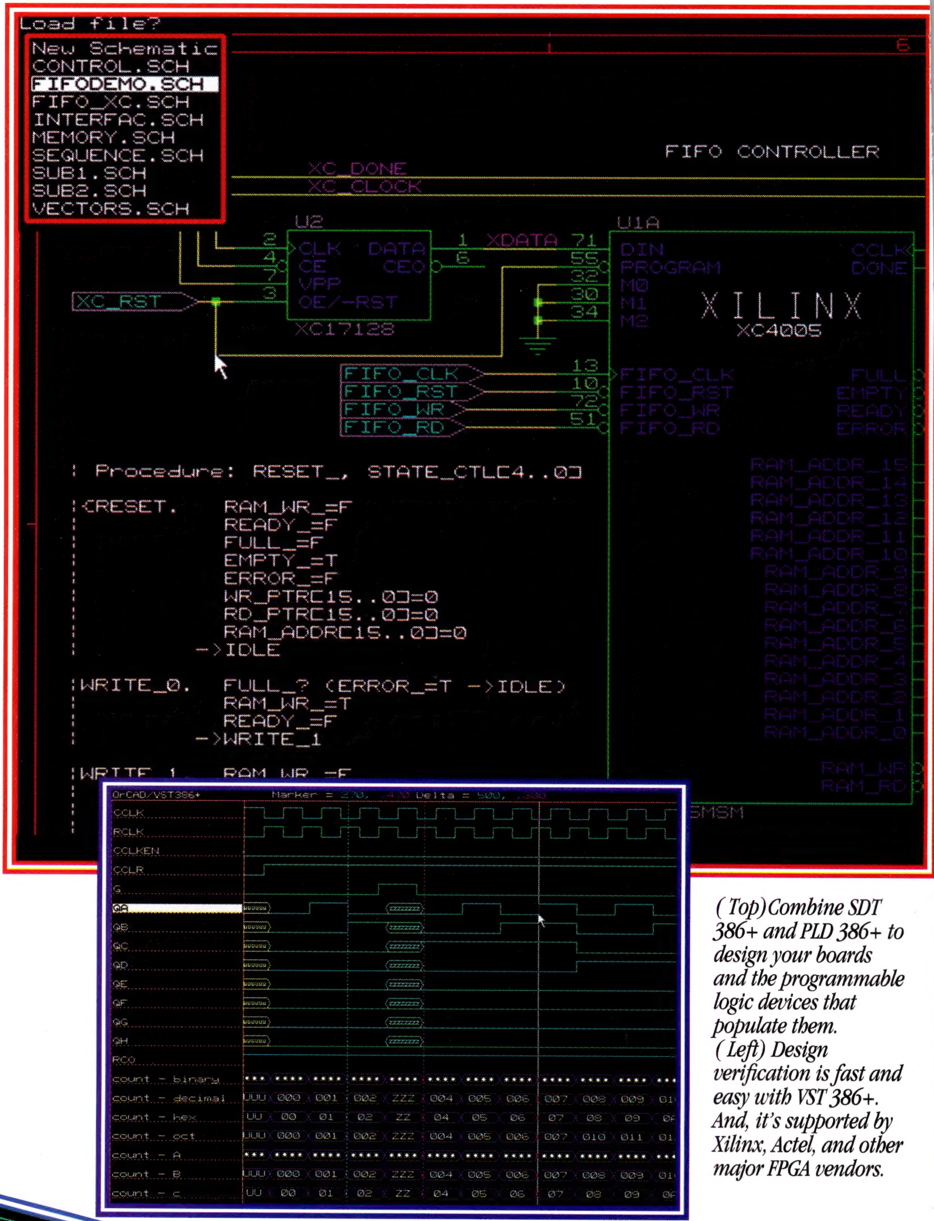

```
: Procedure: RESET_, STATE_CTL[4..0]

:<RESET.     RAM_WR_=F
:            READY_=F
:            FULL_=F
:            EMPTY_=T
:            ERROR_=F
:            WR_PTR[15..0]=0
:            RD_PTR[15..0]=0
:            RAM_ADDR[15..0]=0
:         ->IDLE

:WRITE_0.    FULL_? (ERROR_=T ->IDLE)
:            RAM_WR_=T
:            READY_=F
:         ->WRITE_1

:WRITE_1     RAM_WR_=F
```

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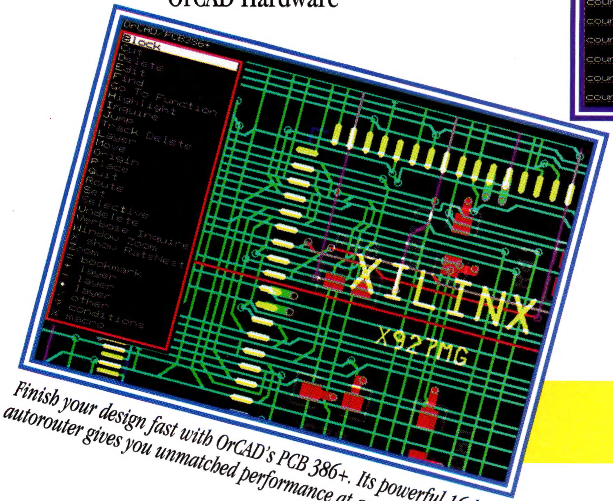

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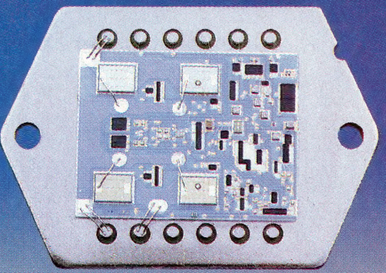

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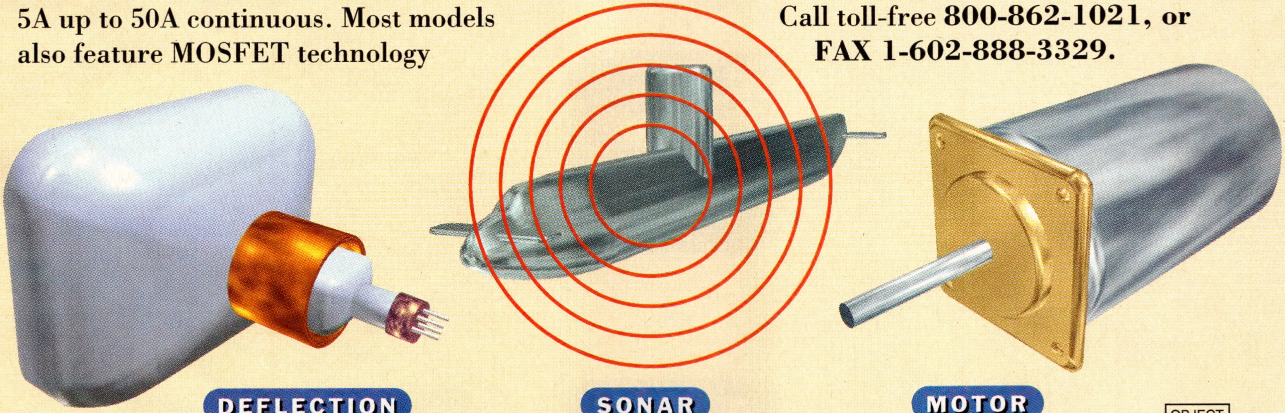

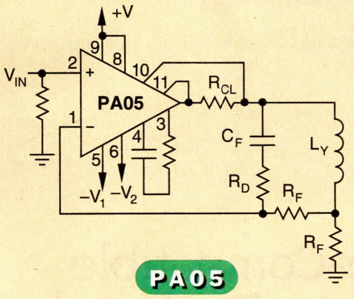

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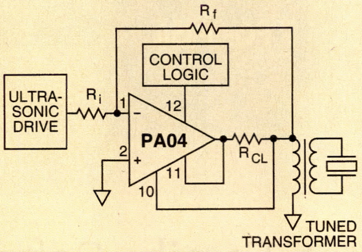

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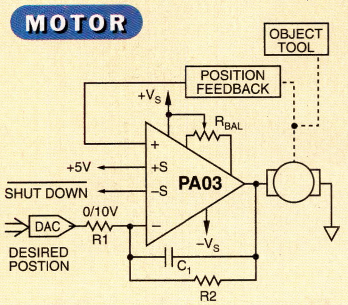

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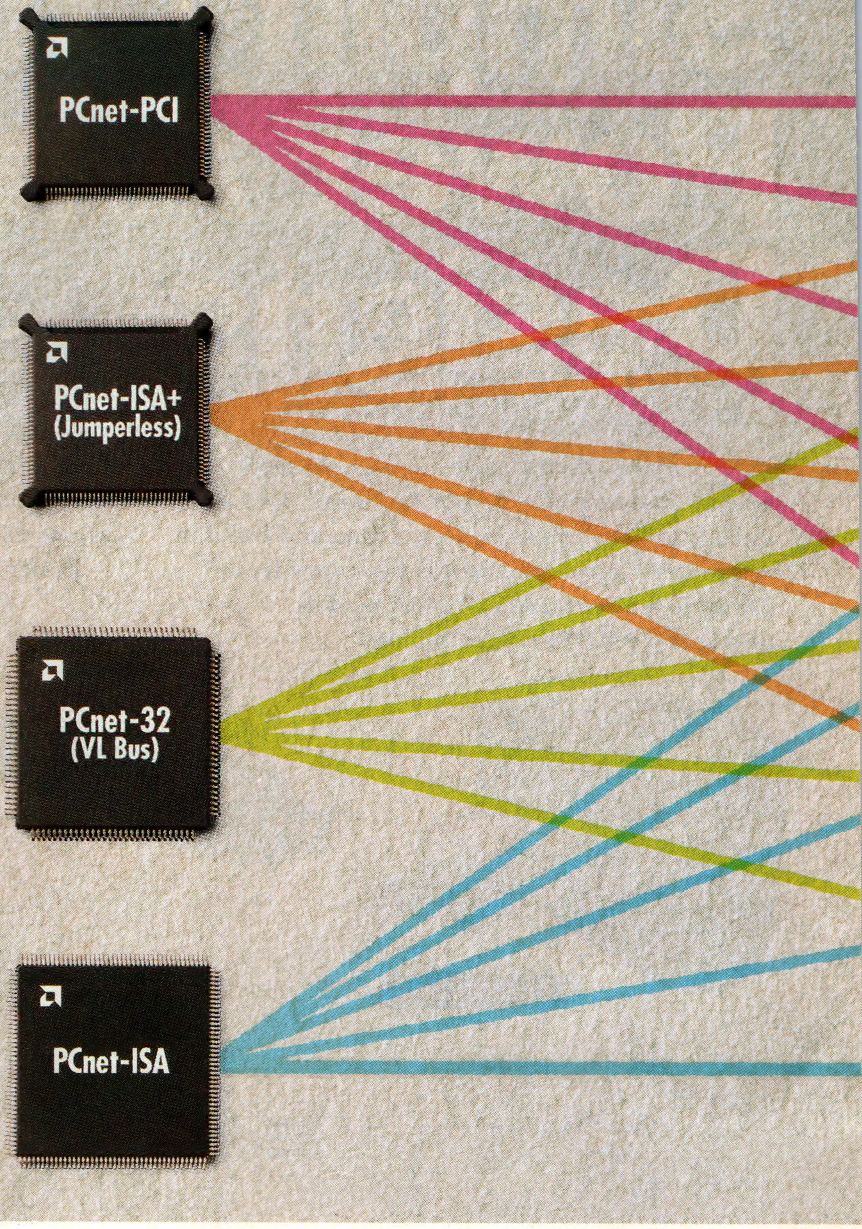

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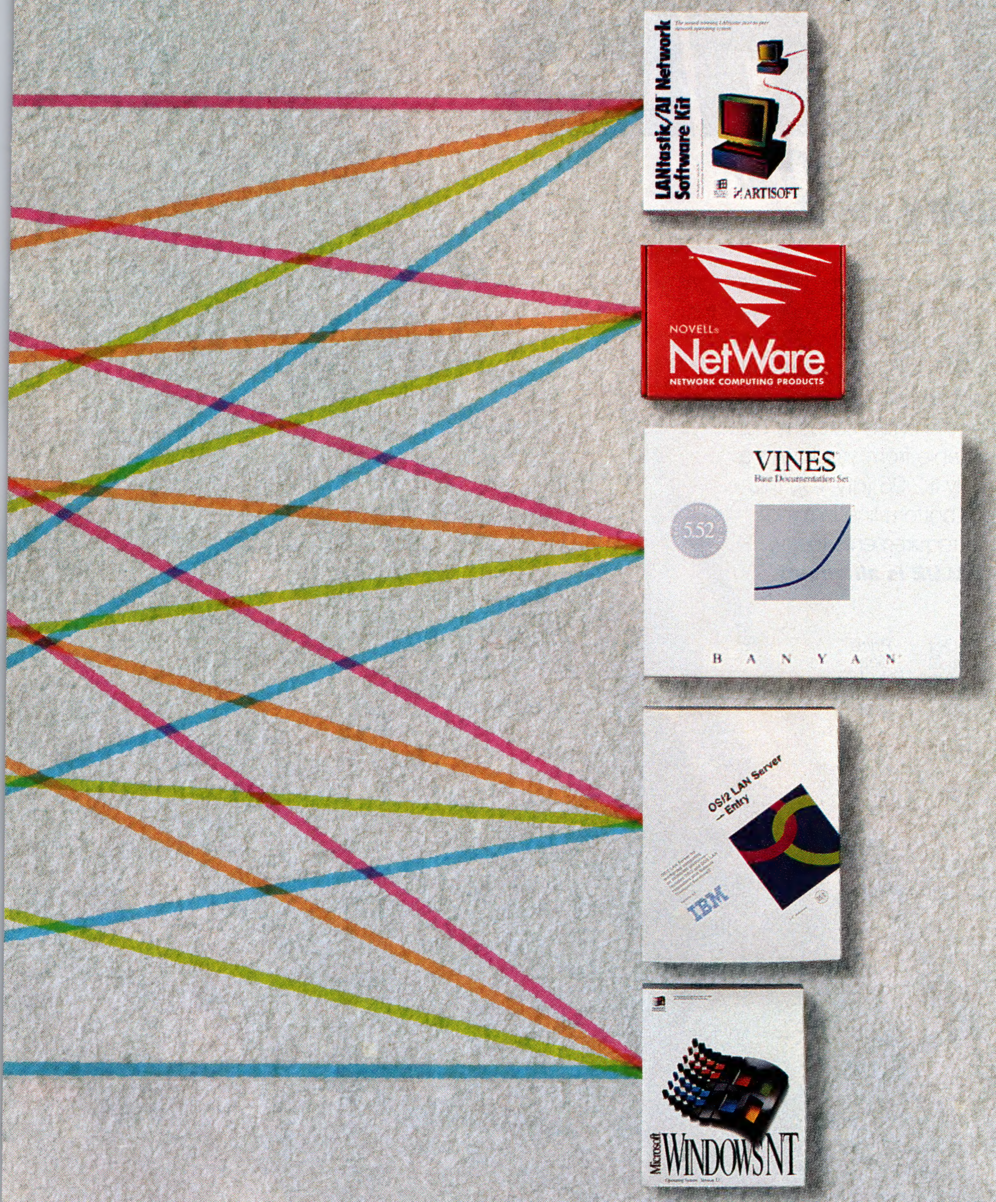

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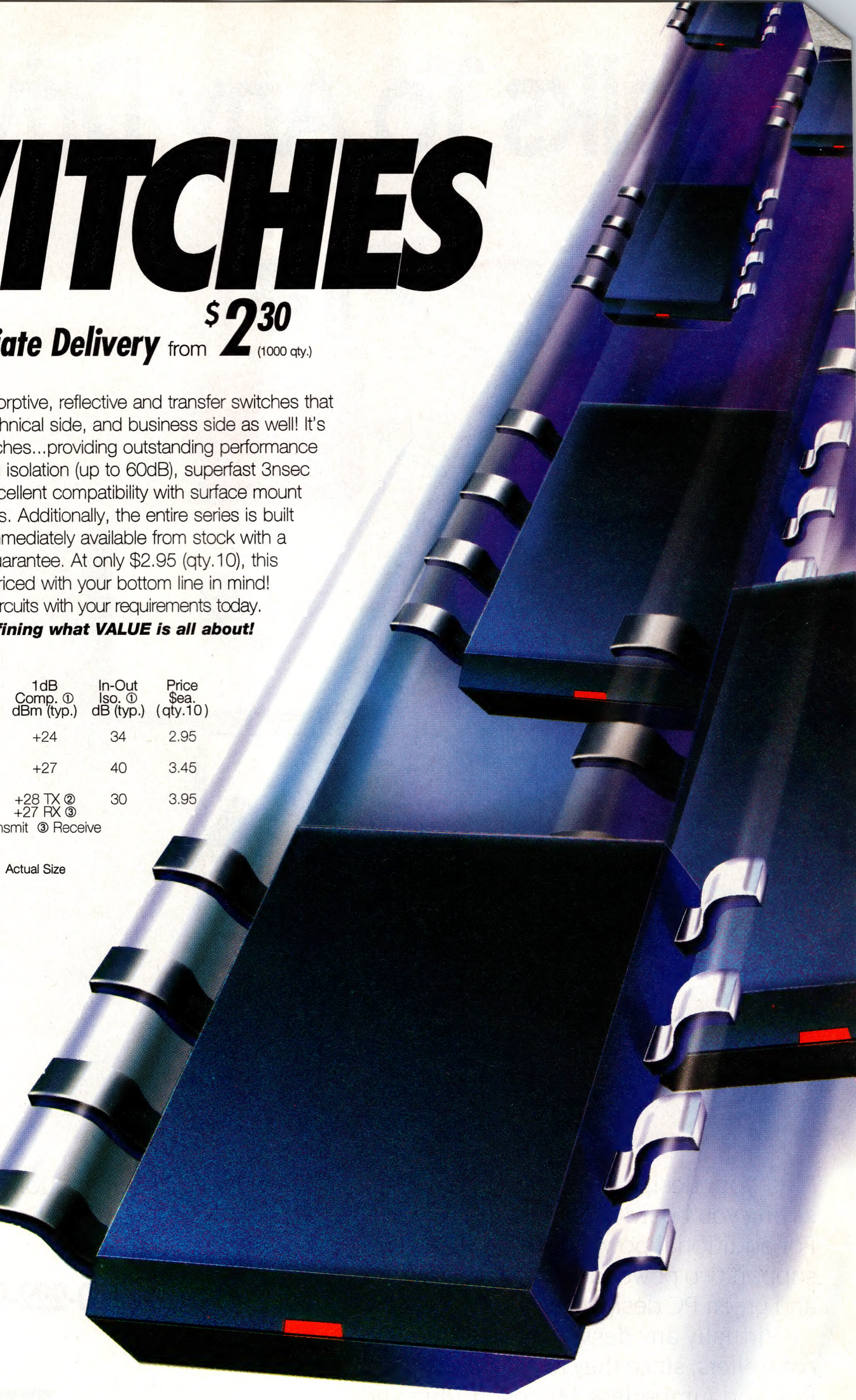

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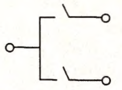

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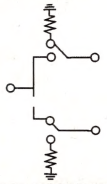

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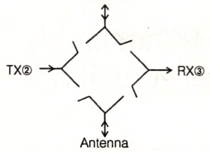

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APRIL 4, 1994 VOL. 42, NO. 7

ELECTRONIC DESIGN

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ELECTRONIC DESIGN

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1972 Certificate of Merit
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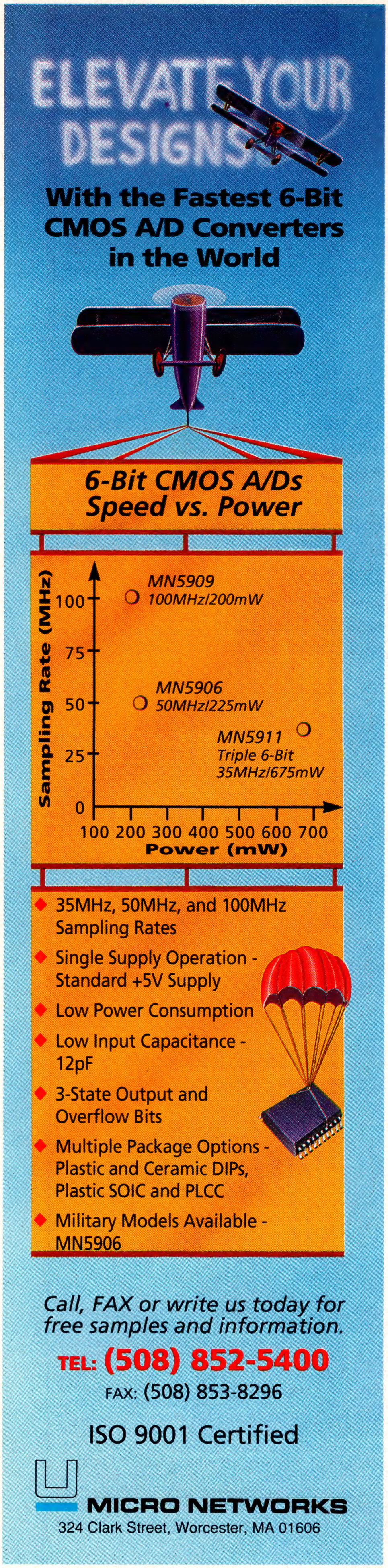

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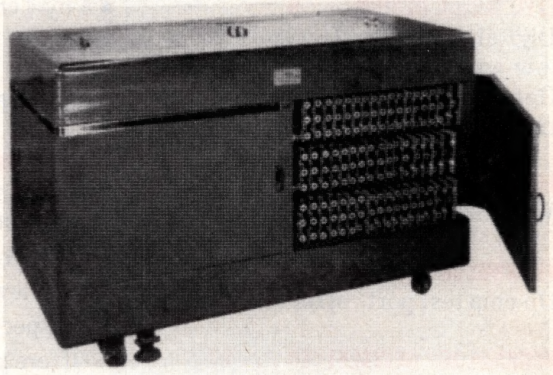

Despite the power consumption—3.5 kW for this one—digital computers were beginning to find real applications in 1954 (see the next item).—SS

New Literature: General purpose computer

The "ERA 1103" General Purpose Computer System is described in an 8-page, 2-color bulletin. This system is a general-purpose digital computer type for applications requiring a large storage capacity and great programming versatility. In addition to performing large scale calculations, the system is adaptable to a wide variety of applications, including simulation and control in real time. Internal memory consists of 17,408 registers, individually addressed and directly accessible. Supplementary storage is provided by four magnetic tape units. Engineering Research Associates, Div. of Remington Rand, Inc., 315 4th Ave., New York 10, N.Y. *(Electronic Design, February 1954, p. 79.)*

One of the first installations of the ERA 1103 computer was at the Air Force's Arnold Engineering Development Center, Tullahoma, Tenn., a wind-tunnel and jet-engine test facility set up in the early 1950s. The AEDC had three 1103s to process the data collected by various transducers in the test chambers. Engineering Research Associates was based in the Twin Cities, Minnesota area, a major center for digital computing technology (the New York address probably was the corporate headquarters for Remington Rand). In addition, the ERA staff published one of the first books on digital computers.—SS

Electronic salesman

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"A machine that talks at the sight of a human being." Fortunately, as stated, it could only give a two-minute sales spiel.—SS

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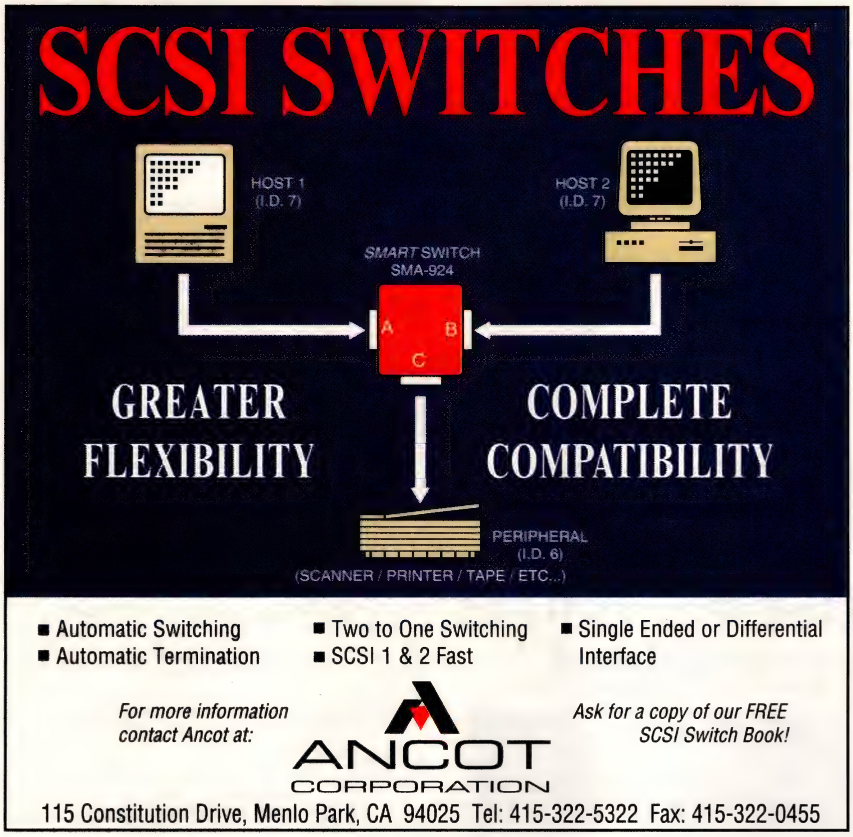

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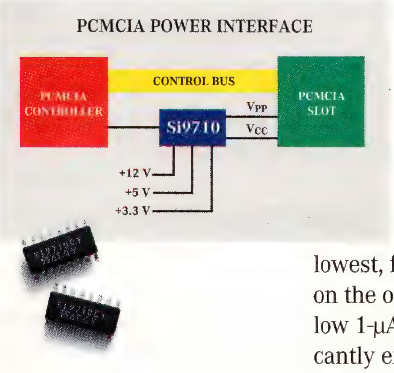

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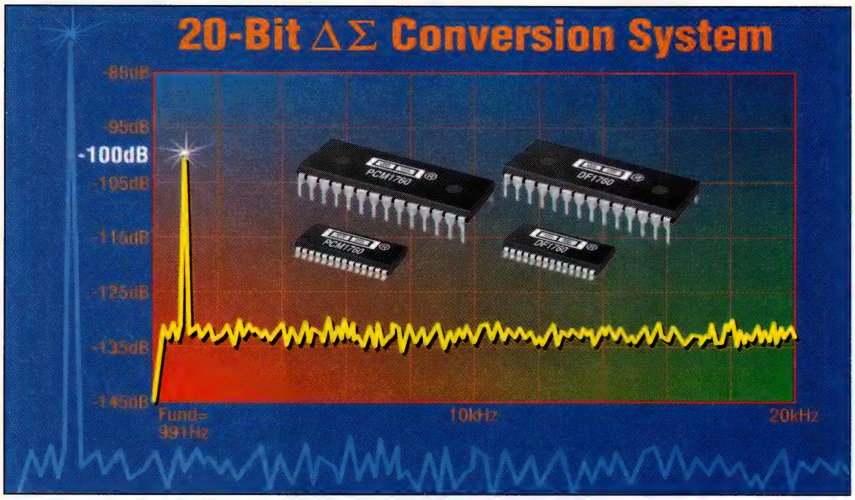
New Product Update

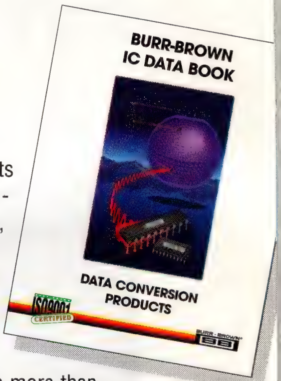


New 20-Bit Digital Audio ADC System

PCM1760 stereo delta-sigma modulator, together with its matched DF1760 digital filter, provide professional digital audio designers the best combination of analog-to-digital converter performance available for under $30! The system offers 20-bit resolution, wide 108dB dynamic range, very low –92dB THD+N, and clear 110dB SNR. PCM1760 and DF1760 are available in 28-pin DIP and SOIC. PCM1760 operates from ±5V supplies, DF1760 from a single 5V supply.

READER SERVICE 198

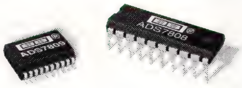
New Data Conversion Products IC Data Book



The Data Conversion Products IC Data Book contains complete product descriptions, specifications, applications tips, and ordering information for a broad line of high performance, high quality data conversion products. With over 950 pages, it offers more than 25 new high performance data conversion solutions. New products profiled include: A/D and D/A converters, data acquisition components, sample/hold amplifiers, V/F converters, multiplexers, and demonstration boards. The Data Conversion Products Data Book is **FREE** from any Burr-Brown sales office or representative.

READER SERVICE 199

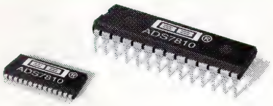
New



12- and 16-Bit Serial Out, 100kHz Sampling A/Ds

ADS7808 and ADS7809 are low cost, general purpose, serial output, CMOS sampling A/Ds. Both deliver 100kHz sampling rates with very low 100mW power dissipation using a single +5V supply. Ideal for many low power, portable applications requiring high sampling rates with superior accuracy and spectral purity, they're perfect for spectrum analyzers, portable oscilloscopes and vibration analyzers, medical electronics, and process control applications—where their serial output simplifies needed isolation. Available in 20-pin 0.3" plastic DIPs and SOICs.

READER SERVICE 200



New 12-Bit, Low Power, 800kHz Sampling A/D

ADS7810's 800kHz sampling rate makes it the world's fastest, 12-bit, monolithic SAR ever—60% faster than its closest competitor! Its high speed, small size, low power, low cost, and excellent Nyquist performance make it ideal for data acquisition, DSP boards, and image processing/scanning applications. Key specs include: 800kHz min sampling rate, 12 bits resolution, 70dB min SINAD with 250kHz input, ±0.5LSB max INL, ±0.9LSB max DNL, and 250mW max power dissipation. Available in 28-pin 0.3" plastic DIP, SOIC and die.

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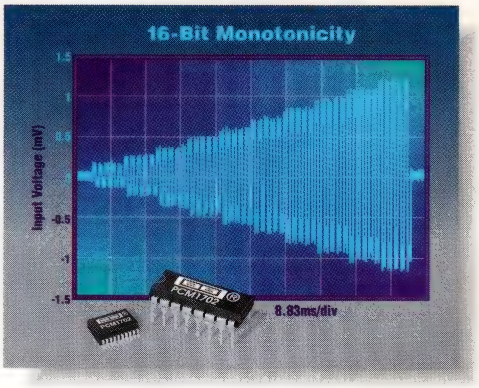

20-Bit BiCMOS DAC

PCM1702's unique architecture produces a 20-bit DAC with high dynamic range, high SNR, and very low distortion. Processed using BiCMOS technology, it has very low power consumption and is packaged in a compact 16-pin plastic DIP or 20-pin SOP. PCM1702 is an unbeatable choice for high-end CD players, musical instrumentation and professional audio applications. Key specs include: –96dB max THD+N, 104dB typ dynamic range, 110dB typ SNR, 200ns typ settling time, and 150mW typ power dissipation.

READER SERVICE 202

New

+5V Voltage Reference Guarantees Long-Term Stability

REF05 is a precision +5V voltage reference that's a pin for pin replacement for the industry standard REF-05. Its guaranteed long-term output voltage drift of 25ppm/1000 hours max is 4 times more stable over extended use than the closest competitor. Key specs are: +5V ±0.1% max output voltage, 8.5ppm/°C max temperature stability, 10µVp-p (0.1Hz to 10Hz) noise, 0.008% max line regulation, 0.005%/mA max load regulation, 1.4mA max quiescent current, and 8VDC to 40VDC supply range. Available in an 8-lead hermetic TO-99.

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New Product Update

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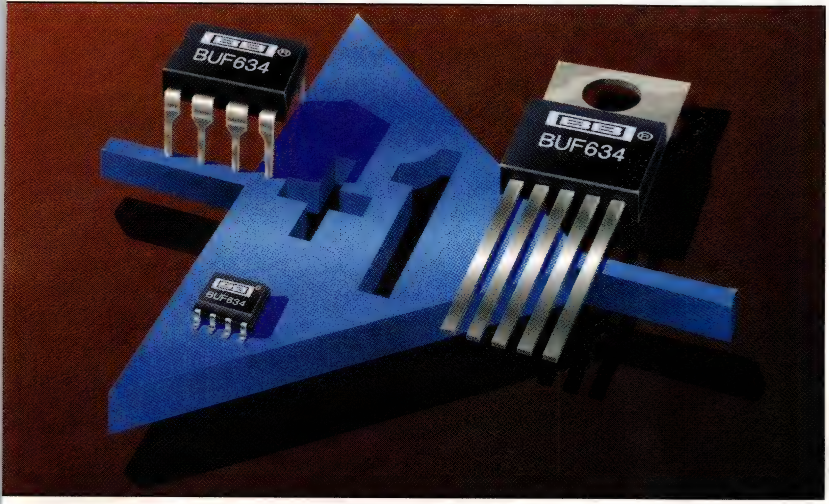


New 250mA Buffer Amp Slews at 2000V/µs

BUF634 is a high speed, unity-gain buffer amplifier that delivers 250mA output and 2000V/µs slew rate—all in a tiny SO-8 package. Its low price, high performance, rugged monolithic design, and ease of use make BUF634 ideal for a wide range of general purpose applications. It's an excellent driver for valves, solenoids, video, and even headphones. BUF634 comes in three different packages: an SO-8 surface mount, an 8-pin plastic DIP, and a 5-pin TO-220.

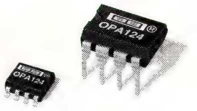
READER SERVICE 204

New Linear Products IC Data Book

The Linear Products IC Data Book contains complete product descriptions, specifications, applications tips, and ordering information for a broad line of high performance, high quality linear products. Its 1100+ pages give designers more than 30 new high performance linear ICs. New products profiled include: operational amplifiers, instrumentation amplifiers, isolation products, power operational amplifiers, references, regulators, and demonstration boards. The Linear Products Data Book is **FREE** from any Burr-Brown sales office or representative.

READER SERVICE 205

New



Low Noise, Precision *Difet*® Op Amp

OPA124 is a precision, monolithic FET op amp that delivers low bias current, noise, voltage offset, and drift plus high open loop gain and common mode rejection. Its versatility, small size, and low price make it ideal for analytical and laboratory instrumentation, data acquisition, test/medical equipment, and optoelectronics. Key specs include: 6nV/$\sqrt{\text{Hz}}$ (10kHz) voltage noise, 1pA max bias current, 2µV/°C max drift, 120dB min open loop gain, 100dB min common mode rejection, and 250µV max offset. Available in compact 8-pin surface mount and plastic DIP packages.

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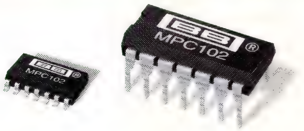
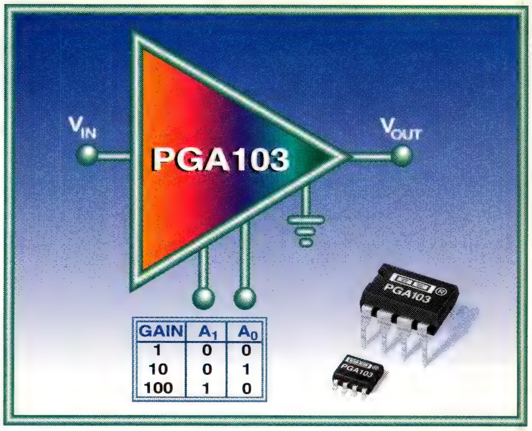


2 x 1 Dual, Video Multiplexer

MPC102 is a dual, 2 x 1 signal multiplexer that distributes and routes wideband analog and digital signals at a high data rate. Designed for high-definition television and broadcast equipment, its excellent harmonic and dynamic specifications are also ideal for radar, communications, computer graphics, and data acquisition systems applications. Key specs include: 210MHz (1.4Vp-p) bandwidth, 640V/µs (2Vp-p) slew rate, 68dB channel crosstalk (30MHz), +6mV/–8mV switching transients, and ±4.6mA (one channel)/±230µA (no channel) quiescent current. Operating from a ±5V supply, MPC102 is available in 14-pin DIPs, SOICs, and dice.

READER SERVICE 207



GAIN	A_1	A_0
1	0	0
10	0	1
100	1	0

New "Easy-to-Use" Programmable-Gain Amplifier

PGA103 is a monolithic digitally programmable amplifier available in an 8-pin plastic DIP and SO-8 surface mount packages. Gains of 1, 10, and 100 are digitally selected by two TTL- or CMOS-compatible control lines. It's an "easy-to-use" simple solution for systems that handle wide dynamic range signals. PGA103's precision, versatility, size, and low cost make it ideal for process control, medical instrumentation, test/measurement equipment, and general-purpose analog boards. Dice also available.

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New

Dual, Isolated, Bi-Directional Digital Coupler

ISO150 is an ultra high-speed capacitively coupled digital device that provides high isolation with very low power consumption. Designed to replace optocouplers, its low power, high speed, and low cost make it a reliable alternative. Use it for A/D and D/A conversion, multiplexed data transmission, computer-to-peripheral interfaces, I/O port isolation in instruments, power inversion, and isolated data acquisition systems. Key specs are: 80M Baud typ data rate, TTL/CMOS compatibility, 25mW max power consumption per channel, tested at 2400Vrms isolated partial discharge per VDE0884, and 16.5mm creepage distance. Available in 24-pin single-wide plastic DIP.

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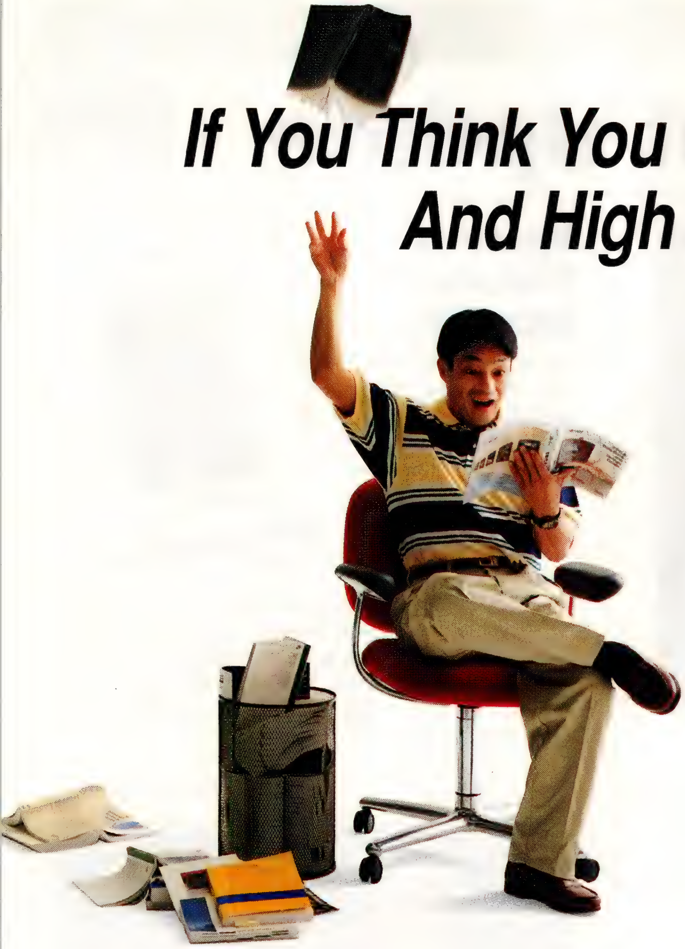
If You Think You Can't Get Both High Speed And High Capacity In An FPGA...



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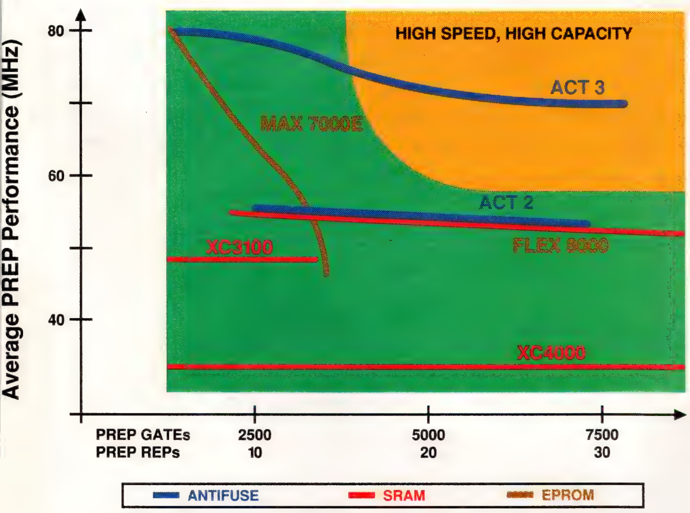

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	Average PREP Performance*			Clock-to-Out
	Fastest	Slowest	Predictability	(Pad-to-Pad)
ACT 3	78 MHz	70 MHz	90%	7.5 ns
FLEX 8000	57 MHz	46 MHz	78%	10.5 ns
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READER SERVICE 174

WAR GAMES

At a time when major segments of our industry are trying valiantly to reinvent themselves to keep pace with the historic shift in the U.S. from a thinly-veiled war economy to a manifestly commercial economy, it seems to me that we should also give some thought to reinventing our industry's metaphors. Terms such as "dogfight," "battle," and "blitz" at best describe only one aspect of being in the electronics business in the 1990s. There is competition, and it is healthy. Cooperation is increasing, and I believe that's often healthy, too.

Because war-games terminology invests otherwise peaceful activities with drama, it's not surprising that journalists and marketing mavens are largely responsible for its use. I can't speak for the marketing community, but we journalists are beginning to change our tone.

Scanning the headlines of your average trade-press publication, for example, uncovers far more "signs pact" and "makes alliance" stories than you would have seen even a few years ago. This isn't necessarily a conscious choice on the part of the editorial community; we're simply reporting more and more instances of cooperative practices.

As a newspaper reporter, I once had a colleague chuckle at the suggestion of a "media conspiracy" to accomplish any goal, worthy or unworthy. "Ridiculous," he'd always say, "the media is too disorganized to have a conspiracy." Or, for that matter, to create a new metaphor for "coop-atition" (cooperation and competition).

Engineers, on the other hand, are as well versed as any profession in the synergy created between cooperation and competition. The friendly venue of a technical conference, for example, provides a competitive field in the realm of ideas. Companies send engineers to conferences to find out if their ideas are flawed. The development costs of flawed products that were never built can be plowed into other products: a net win for the industry's economy.

Certainly the use of war-games metaphors is decreasing. To me, though, the fact that we haven't invented a group of replacement metaphores means that the coop-atition idea is still immature.

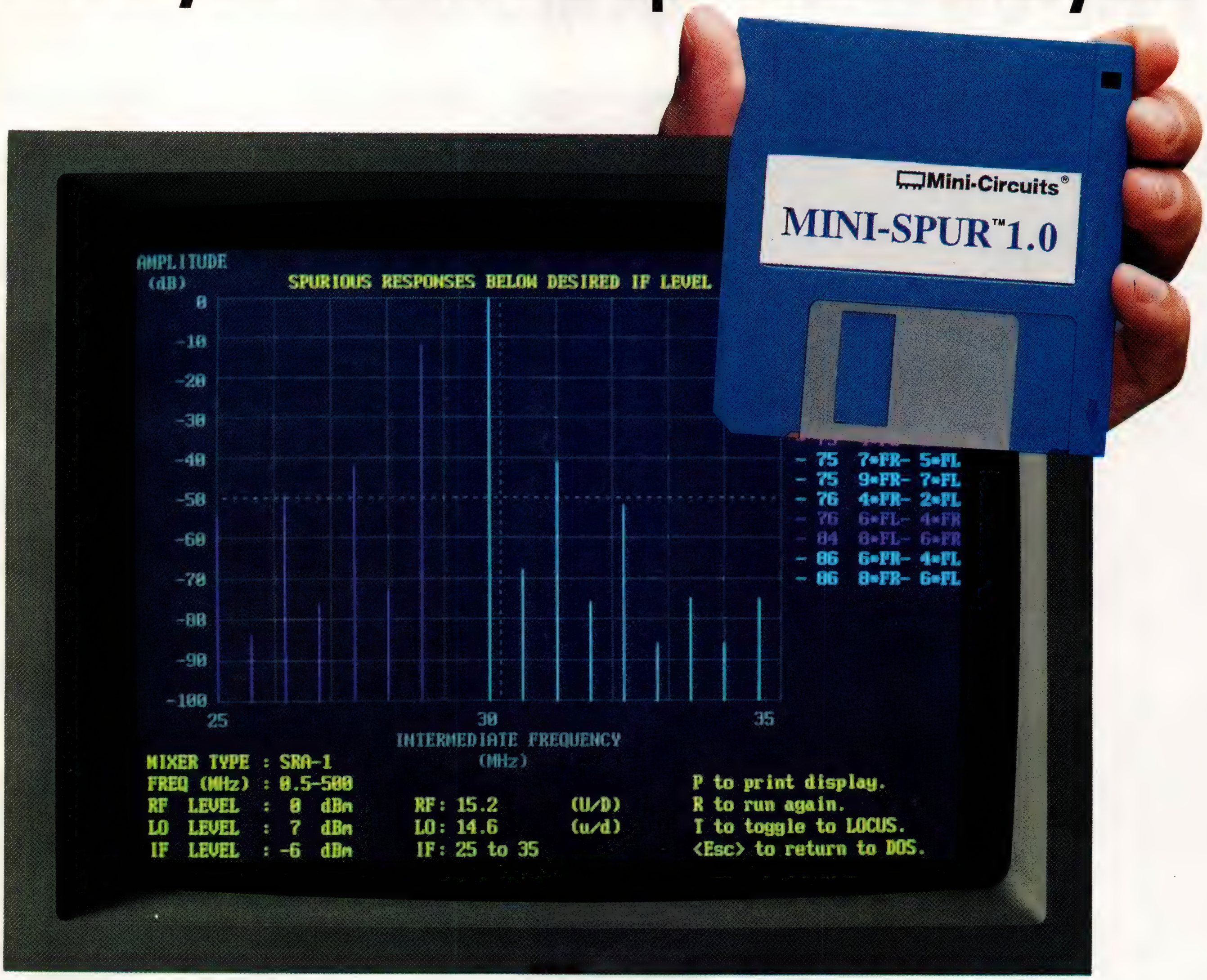
Inventing new metaphores is difficult because it requires us not just to talk and write in a new way, but to think in a new way. Nevertheless, I think it is important and worthwhile.

Should we look to the world of diplomacy (foggy bottom) for a new paradigm? I think not. The power of words is that they reflect and create images of what we are. Right now, we're in between two worlds and that's always a bit uncomfortable to say the least.

Josh Shandle
Editor-in-Chief

Mini-Spur™ 1.0

turns your PC into a Spectrum Analyzer *



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- 75  7*FR- 5*FL
- 75  9*FR- 7*FL
- 76  4*FR- 2*FL
- 76  6*FL- 4*FR
- 84  8*FL- 6*FR
- 86  6*FR- 4*FL
- 86  8*FR- 6*FL

MIXER TYPE : SRA-1
FREQ (MHz) : 0.5-500                                P to print display.
RF  LEVEL  :  0  dBm     RF: 15.2        (U/D)       R to run again.
LO  LEVEL  :  7  dBm     LO: 14.6        (u/d)       T to toggle to LOCUS.
IF  LEVEL  : -6  dBm     IF: 25 to 35                <Esc> to return to DOS.
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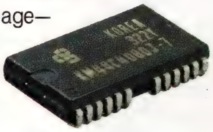
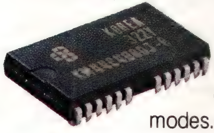


Samsung's 16M DRAMs have been optimally designed in x1/x4 and x8/x16 chip sets with fast access times of 50/60/70ns. A new extended data output(EDO)mode enhances access times over chips that use conventional fast page modes. Moreover, these chips are extremely energy efficient, drawing not 5volts, but a mere 3.3volts of power.



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4MX 4	Fast Page	KM44C(V) 4000A/AL/ASL/ALL KM44C(V) 4100A/AL/ASL/ALL	4096Cycle/64ms 2048Cycle/32ms
	Static Column	KM44C(V)4002A/AL/ASL/ALL KM44C(V)4102A/AL/ASL/ALL	4096Cycle/64ms 2048Cycle/32ms
	Quad-$\overline{CAS}$	KM44C(V)4003A/AL/ASL/ALL KM44C(V)4103A/AL/ASL/ALL	4096Cycle/64ms 2048Cycle/32ms
	EDO(Hyper Page)	KM44C(V)4004A/AL/ASL/ALL KM44C(V)4104A/AL/ASL/ALL	4096Cycle/64ms 2048Cycle/32ms
2MX 8	Fast Page	KM48C(V) 2000A/AL/ASL/ALL KM48C(V)2100A/AL/ASL/ALL	4096Cycle/64ms 2048Cycle/32ms
1MX16	Fast Page	KM416C(V)1000/L/LL KM416C 1200/L/LL	4096Cycle/64ms 1024Cycle/16ms
1MX 4	Fast Page Static Column Quad-$\overline{CAS}$ EDO(Hyper Page)	KM44C(V)1000C/CL/CSL/CLL KM44C(V)1000C/CL/CSL/CLL KM44C(V)1003C/CL/CSL/CLL KM44C(V)1004C/CL/CSL/CLL	1024Cycle/16ms 1024Cycle/16ms 1024Cycle/16ms 1024Cycle/16ms
4MX 1	Fast Page Static Column EDO(Hyper Page)	KM41C(V)4000C/CL/CSL/CLL KM41C(V)4000C/CL/CSL/CLL KM41C(V)4004C/CL/CSL/CLL	1024Cycle/16ms 1024Cycle/16ms 1024Cycle/16ms

- 'V' in Part No. means 3.3V part

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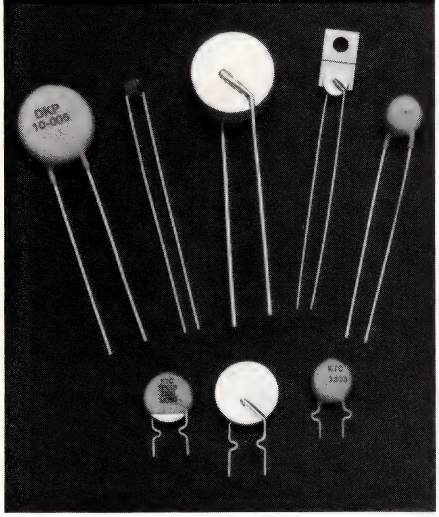

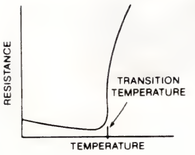

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READER SERVICE 116

ON-CHIP TEST PORTS OFFER A HAVEN

Help may be on the way for designers of complex microprocessor-based systems whose densities make them difficult and costly to probe and debug. The aid comes in the form of test access ports built on microprocessors to support emulation and debug systems. Although such ports have already proven their usefulness, their ultimate success may hinge on whether the industry can agree to standardize the functions and protocols used by the ports.

One obvious implementation is the IEEE-1149.1 boundary-scan JTAG test access port. The problem is the lack of standardization in building the required additional functionality into the JTAG port. Even divisions within the same chip company have come up with different versions, according to Brian Crowley, director of engineering at Applied Microsystems Corp., Redmond, Wash. That creates a problem for both his emulator designers and customers. "Our emulators are embedded systems themselves," says Crowley. "We have the same problems that everybody else has when it comes to probing boards. So it would be nice if there was some uniform way of going about it."

JOHN NOVELLINO
TEST & MEASUREMENT

Although the actual implementations vary widely, the basic concept is similar. The ports use pins dedicated to testing to create a serial I/O channel into the device. "When the device is operating, those pins are not serving any other practical purposes," says Gary Richmond, product marketing manager for logic-analyzer microprocessor support at Tektronix, Beaverton, Ore. "So the thought is, why not use them to get access to what is going on inside the chip while it's running."

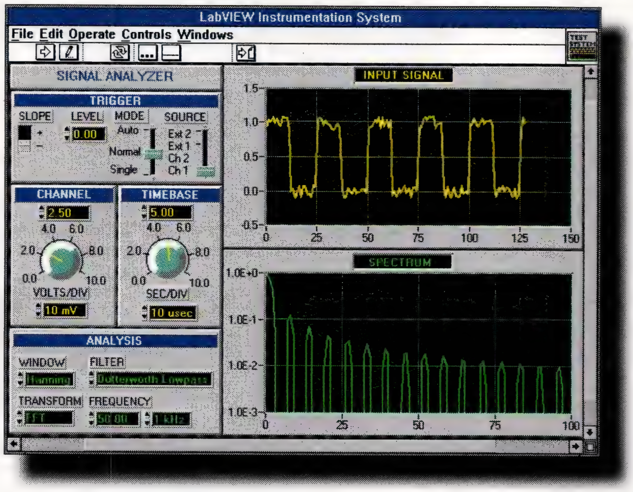
The four-pin JTAG port is being placed on many chips to solve the probing problem inherent in interconnect testing of high-density boards. "The main benefit of the JTAG port is that it's a four-wire connection and easy to tap into as opposed to connecting a probe and having to sell configuration registers and things like that in an emulator," says Dave Cipriani, product marketing engineer for logic analyzers and emulators at Hewlett-Packard's Colorado Springs Div.

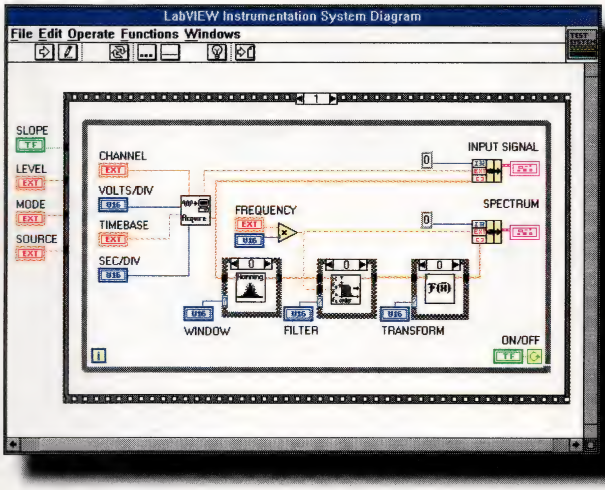
But a straight JTAG port does little to help when emulating and debugging microprocessor systems. It's completely outside the realm of IEEE-1149.1. Therefore, CPU designers must add functionality to the IC if the JTAG port is to significantly aid emulator designers—and users. The port could then be used to examine and change the contents of registers; start, stop, and single-step the microprocessor; and download code. About the only emulator function the port can't handle is real-time trace of code, due to the limits of the serial output.

An example of a successful port completely divorced from the JTAG version is the eight-pin Background Debug Mode (BDM) port developed by Motorola. The port was a critical factor is allowing Nohau Corp., Campbell, Calif., to build a relatively low-cost debugger for the 68300 and 68HC16 series chips, says Randy Devol, product manager. "Ports like the BDM port from Motorola are, I think, a great example of how chip design can include concepts important to the development process," says Devol. He also notes that to simplify emulator design and manufacturing, Intel supplies emulator vendors with bond-out chips containing extra pins not found on production parts.

Because of the success of the bond-out parts and the BDM port, Devol expects to see more CPUs with dedicated debugging pins. Indeed the fact that chip vendors are now willing to devote some of their valuable silicon area and pin count to test access ports of any kind is an important recognition on their part of the problem that exists with design bebug. "The development process is an essential part of selling chips," Devol says. "If you build a chip that is more difficult to design into a target system and debug in a target system, you're going to sell fewer chips."

More than Just Ease of Use ...





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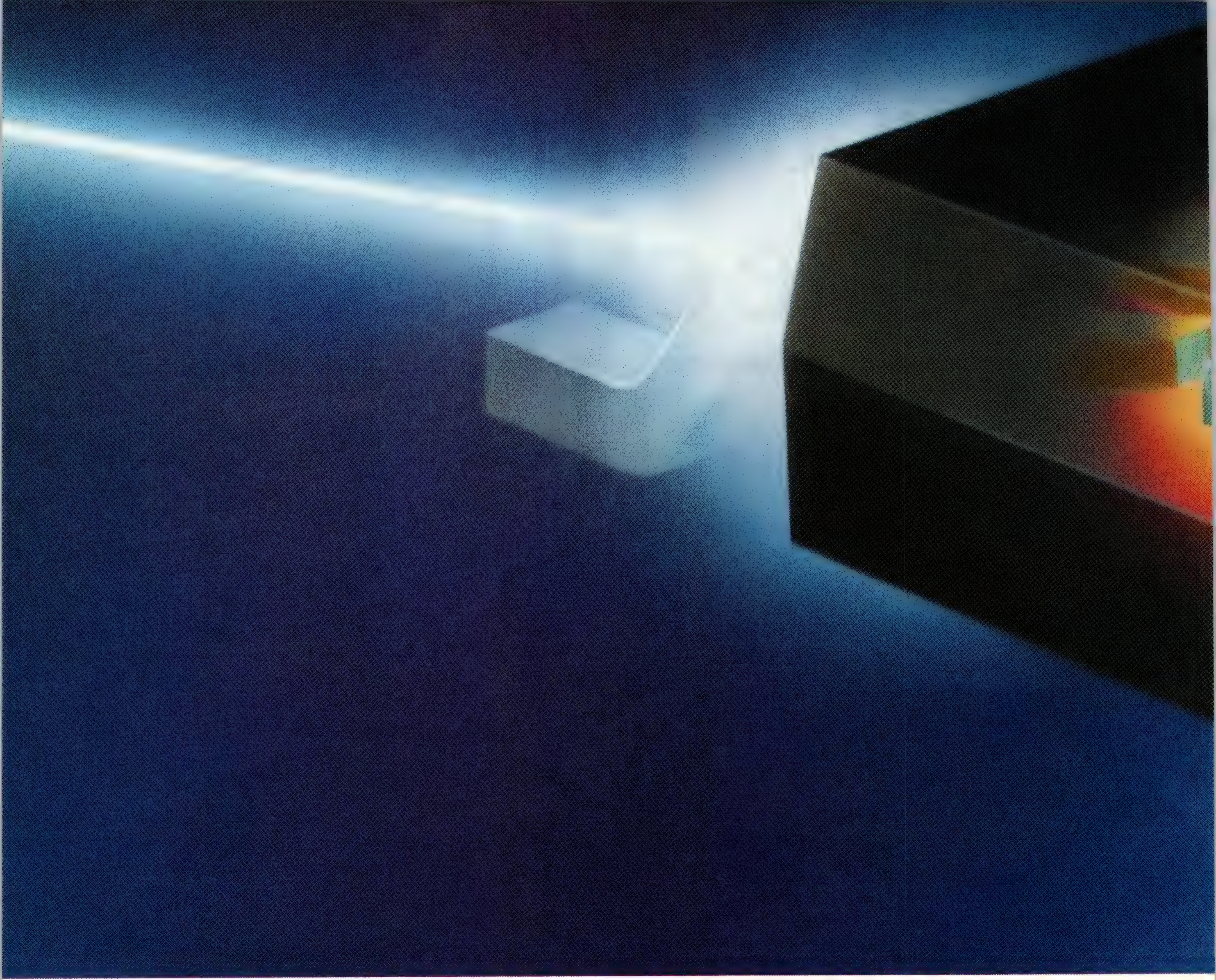

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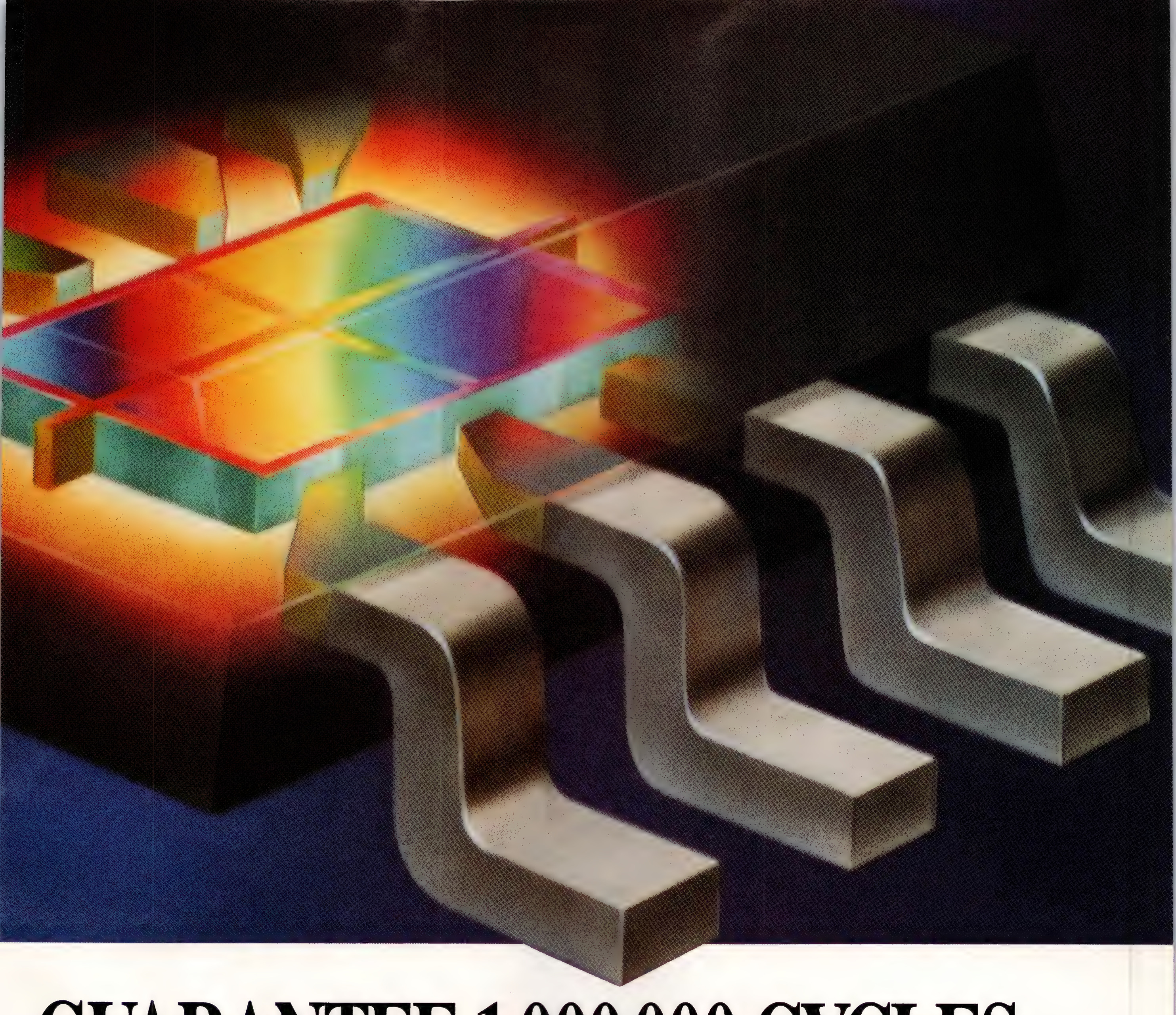
PARALLEL								64K	256K

COMING SOON



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Power-full tiny inverter.

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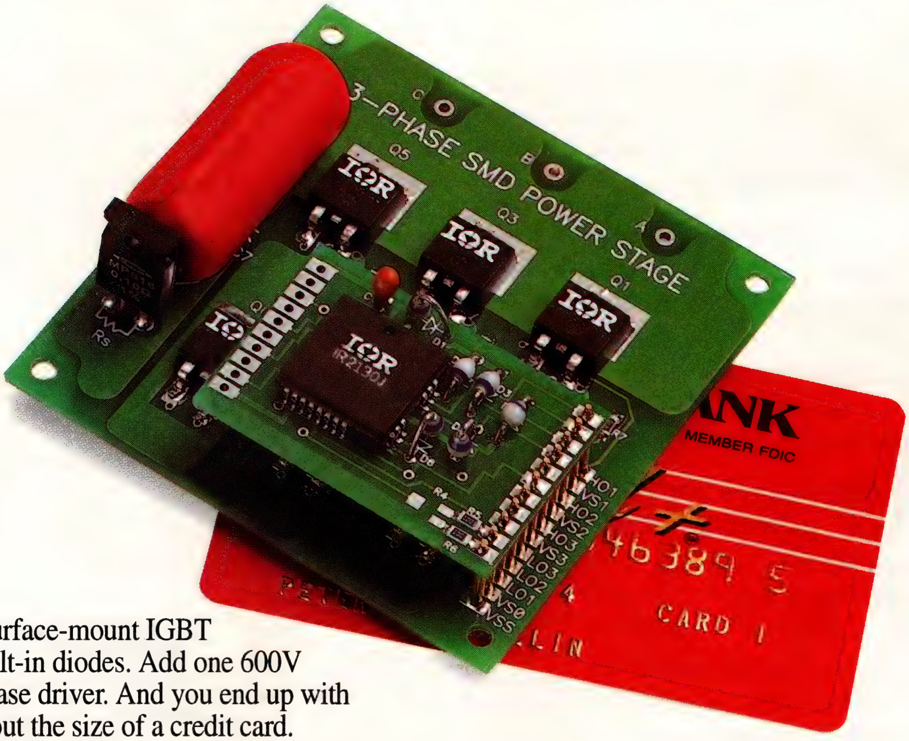

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TECHNOLOGY NEWSLETTER

3D MULTICHIP MODULE TO BE DEMONSTRATED

As the result of a U.S. Air Force research-and-development contract, a new type of package that incorporates varying sizes and types of chips and chip stacks into a single assembly will be demonstrated. Irvine Sensors Corp., Costa Mesa, Calif., will construct what it calls a multi-modular computer module (MMCM) to demonstrate its ability to provide manufacturers and system users with a standardized modular structure for high-level integration of its chip stacks. The MMCM will be fabricated from a series of interconnected ceramic building blocks with enclosed wells in which chip stacks or specialized chips can be mounted hermetically. Use of such blocks would permit heterogeneous assemblies of various types of memories, processors, FPGAs, and ASICs to be housed in an extremely compact space. Such a structure could facilitate rapid development of advanced systems through the use of mix-and-match modular elements. Initial Air Force interest stems from the desire to fit vibration-resistant electronics into highly constrained cylindrical forms like missiles and missile interceptors. Call Irvine Sensors at (714) 549-8211. *DM*

STANDARD OFFERS PDA CORDLESS CONVENIENCE

The Infrared Data Association, IrDA, has announced the first release of a noninterfering, interoperable, worldwide infrared connectivity standard for data devices. Many of today's mobile systems with IR capabilities, such as Newton and Omnibook, don't easily connect with each other or other complementary devices. The IrDA standard will specifically address this problem by allowing quick and dependable exchanges of data files between a host of electronic devices. Assuming each device recognizes the same data types, any product type or brand name device will be able to exchange information. Currently, all physical and protocol levels—serial infrared (SIR), infrared link-access protocol (IRLAP), and the link-management protocol—have been placed before the IrDA membership for final comment. Adoption of the completed standard is expected by April 27. In conjunction with the IrDA standard, certification standards and specifications are being developed to verify products prior to being granted the IrDA certification mark. It's anticipated that future applications will utilize low-power IrDA-enabled devices to allow for the exchange of data in an easier and more accessible manner. Copies of the specifications can be obtained in May for a non-member fee of $500. Contact John LaRoche at (510) 943-6546. *CA*

ONE-STOP SHOPPING FOR MOBITEX COMMUNICATIONS

Users of Mobitex, a multi-user wireless data-communication network that provides coverage in top metropolitan areas, may soon have a single and complete source for their communications needs. Granite Communications Inc., Manchester, N.H., and Cyplex Corp., Nashua, N.H., have formed a joint venture that will target those Mobitex users who require both handheld devices and fixed-point equipment, through the integration of Granite's Videopad family of products into new applications in the fixed-data market place. Videopad products include a menu-driven user interface, built-in short-range RF communication, signature capture, and integrated bar-code scanning. The Videopad technology, combined with the wireless data solutions designed and manufactured by Cyplex, promise to offer a wide range of cost-effective solutions to address the needs of Mobitex users. The Mobitex service is operated in the U.S. by RAM Mobile Data, Nashua, N.H. Contact Cyplex's Matt Pierson at (603) 882-8104, ext. 303. *CA*

PROTOTYPING SERVICE JUMPSTARTS PACKAGING

An industry consortium with a broad base of packaging prototyping and manufacturing expertise is offering its services to members and non-members alike. The Microelectronics and Computer Technology Corp. (MCC), Austin, Texas, says that its advanced manufacturing and prototyping service (AMPS) is a way for OEMs to reduce their product-development costs and time to market. Services extend to four key areas: bare-die assemblies for electronic products (rapid prototyping of multichip modules and quick-turn flip-chip and TAB assemblies); back-end processing of IC wafers (wafer bumping with gold, solder, or elastomer bumps; bumped, single die for TAB or flip chip; known-good-die single-die carriers); display components, assembly, and packaging (flip-chip on glass, anode/cathode plates); and high-density interconnect (HDI) substrates (custom, high-frequency, or superconducting HDI substrates). In addition to prototyping and limited manufacturing services, MCC will provide technology analysis and design services as well as assist with technology insertions. Contact MCC's Rick Nolan at (512) 250-3016. *DM*

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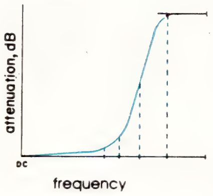
LOW PASS



low pass, Plug-in, dc to 1200MHz

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
★LP-5	DC-5	8-10	10-200
★LP-10.7	DC-11	19-24	24-200
★LP-21.4	DC-22	32-41	41-200
★LP-30	DC-32	47-61	61-200
★LP-50	DC-48	70-90	90-200
★LP-70	DC-60	90-117	117-300
★P-90	DC-81	121-137	167-400
★LP-100	DC-98	146-189	189-400
★LP-150	DC-140	210-300	300-600
★LP-200	DC-190	290-390	390-800

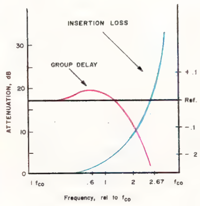
Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
★LP-250	DC-225	320-400	400-1200
★LP-300	DC-270	410-550	550-1200
★LP-450	DC-400	580-750	750-1800
★LP-550	DC-520	750-920	920-2000
★LP-600	DC-680	840-1120	1120-2000
★LP-750	DC-700	1000-1300	1300-2000
★LP-800	DC-720	1080-1400	1400-2000
★LP-850	DC-760	1100-1400	1400-2000
★LP-1000	DC-900	1340-1750	1750-2000
★LP-1200	DC-1000	1620-2100	2100-2500

Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

Surface-mount, dc to 570MHz

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
SCLF-21.4	DC-22	32-41	41-200
SCLF-30	DC-30	47-61	61-200
SCLF-45	DC-45	70-90	90-200
SCLF-135	DC-135	210-300	300-600
SCLF-190	DC-190	290-390	390-800
SCLF-380	DC-380	580-750	750-1800
SCLF-420	DC-420	750-920	920-2000

Price, (1-9 qty), all models: $11.45

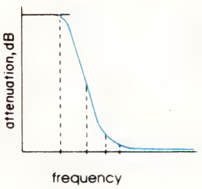


Flat Time Delay, dc to 1870MHz

Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	Stopband MHz loss > 20dB	VSWR Freq. Range, DC thru 0.2fco X̄	VSWR Freq. Range, DC thru 0.6fco X̄	Group Delay Variations, ns Freq. Range, DC thru fco X̄	Group Delay Variations, ns Freq. Range, DC thru 2fco X̄	Group Delay Variations, ns Freq. Range, DC thru 2.67fco X̄
★BLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
★BLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
★BLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
★BLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
★BLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
★BLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

HIGH PASS



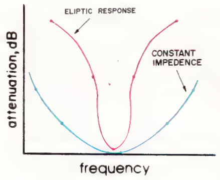
high pass, Plug-in, 27.5 to 2200MHz

Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband, MHz loss < 1dB	VSWR Pass-band Typ.
★HP-25	DC-13	13-19	27.5-200	1.8:1
★HP-50	DC-20	20-26	41-200	1.5:1
★HP-100	DC-40	40-55	90-400	1.8:1
★HP-150	DC-70	70-95	133-600	1.8:1
★HP-175	DC-70	70-105	160-800	1.5:1
★HP-200	DC-90	90-116	185-800	1.6:1
★HP-250	DC-100	100-150	225-1200	1.3:1
★HP-300	DC-145	145-170	290-1200	1.7:1

Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband, MHz loss < 1dB	VSWR Pass-band Typ.
★HP-400	DC-210	210-290	395-1600	1.7:1
★HP-500	DC-280	280-365	500-1600	1.8:1
★HP-600	DC-350	350-440	600-1600	2.0:1
★HP-700	DC-400	400-520	700-1800	1.6:1
★HP-800	DC-445	445-570	780-2000	2.1:1
★HP-900	DC-520	520-660	910-2100	1.8:1
★HP-1000	DC-550	550-720	1000-2200	1.9:1

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

BANDPASS



bandpass, Elliptic Response, 10.7 to 70MHz

Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	Stopbands I.L. > 35dB at MHz
★BP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
★BP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
★BP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
★BP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
★BP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95,
BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
★IF-21.4	21.4	18-25	1.3 & 150	DC-220
★IF-30	30	25-35	1.9 & 210	DC-330
★IF-40	42	35-49	2.6 & 300	DC-400
★IF-50	50	41-58	3.1 & 350	DC-440
★IF-60	60	50-70	3.8 & 400	DC-500
★IF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in $14.95,
BNC $36.95, SMA $38.95, Type N $39.95

NOTE: ★**Add Prefix P, B, N, or S for Pin, BNC, N, or SMA connector requirement.**

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SPEC BREAKS 528-MBYTE DISK-DRIVE BARRIER

An industry specification that overcomes the 528-Mbyte capacity addressing barrier in hard-disk drives is quickly picking up steam. The specification is supported by such companies as Conner Peripherals, IBM, Microsoft, Novell, Phoenix Technologies, Quantum, SCO, Seagate Technology, and Western Digital. To integrate AT-interface disk drives into PCs, the system BIOS and operating system must address each drive's capacity uniformly. Until now, drives with a capacity greater than 528 Mbytes lacked that uniformity. BIOS implementations containing the open specification are available now, and formal standard approval should be granted by the summer. Efforts are still underway to aid users of older systems built with a non-upgradable BIOS. For a copy of the BIOS and disk-drive specifications, contact Tim Sutton of Seagate at (408) 439-2880. *RN*

TOOLKIT CREATES NT TELEPHONY APPLICATIONS

Creating a sophisticated computer telephony service that runs under Windows NT can be quite a complex task for engineers. One development, the OmniVox NT toolkit devised by Apex Voice Communications, Sherman Oaks, Calif., helps in the creation of automated, voice-processing applications that capitalize on such NT features as protocols using dynamic data exchange, named pipes, and mapped files. The object-oriented (C++) graphical tool simplifies developing various telephony applications including audiotex, automated attendant, information delivery, and interactive voice response on hardware from Dialogic Corp., Parsippany, N.J. OmniVox NT also supports open database connectivity for C programs that are linked with enterprise databases. Voice files created using DOS editors are compatible with the OmniVox NT Kit. For more information, call Apex at (818) 379-8400 or (800) 727-3970. *SVT*

SUPERCONDUCTING FILMS SHOW ZERO RESISTANCE

For the first time, researchers have come up with thin films of the superconducting material mercury-barium-calcium-copper oxide that exhibit zero resistance. Scientists at IBM Research Division's Thomas J. Watson Research Center, Yorktown Heights, N.Y., coaxed the films into superconducting at a zero-resistance transition temperature of 124K (–149°C). Because of their excellent electrical and magnetic characteristics, as well as a transition temperature that's almost as high for the material in bulk form, such films are expected to have practical applications in electronic devices. Although thin films of other materials already are used in several electronic applications, they become superconducting at temperatures some 30K cooler. To fabricate the films, the researchers had to overcome problems stemming from the volatile and toxic nature of mercury and mercury oxide. By doing so, they found that the film's critical current density was at least 300 kA/cm^2 at 10K (–263°C) and 50 kA at 77K (–196°C). The first property indicates how sufficient a superconductor the material is, and the second indicates its usefulness in real applications. Considering that the material has yet to be optimized, the scientists are encouraged about the prospects for its practicality. Contact the Research Center at (914) 784-7466. *DM*

WAFER-SCALE ATM SWITCHES BEING FORECAST

The speed and complexity of asynchronous transfer-mode (ATM) communications is compelling technologists to re-explore the promise of wafer-scale integration (WSI). With WSI, entire multichip systems would be fabricated and connected on a single semiconductor wafer. As ATM transmission rates approach the gigabit range, delay times between components become increasingly critical, forcing the need for shorter and shorter lead lengths. The complexity of large ATM switch fabrics also would lead to large, expensive interconnection schemes between switch elements, unless they're integrated sufficiently. A study by Nader Mirfakhraei of the Computer and Communications Research Center at Washington University, St. Louis, Mo., indicates that the cost and complexity of fabricating WSI components for ATM switching could be outweighed by the potential speed advantage and system-level cost savings. The study, underwritten in part by the U.S. National Science Foundation and several leading technology corporations, investigated how WSI might deal with the problems associated with routing large volumes of high-speed digital packets in a switched, variable-bandwidth environment. Besides solving the propagation delay and interconnect issues, the study concluded that WSI could support an innovative type of switching technology. Called the multipath buffered crossbar (MBC), it uses two sets of crosspoints (sharing a common buffer) for each connection to enhance reliability. This architecture also facilitates multicasting of single data streams to multiple destinations, a very desirable characteristic for public-switch components. For further information, contact Nader Mirfakhraei at the Computer and Communications Research Center, Campus Box 1115, Washington University, St. Louis, MO 63130; e-mail: nader@dworkin.wustl.edu. *LG*

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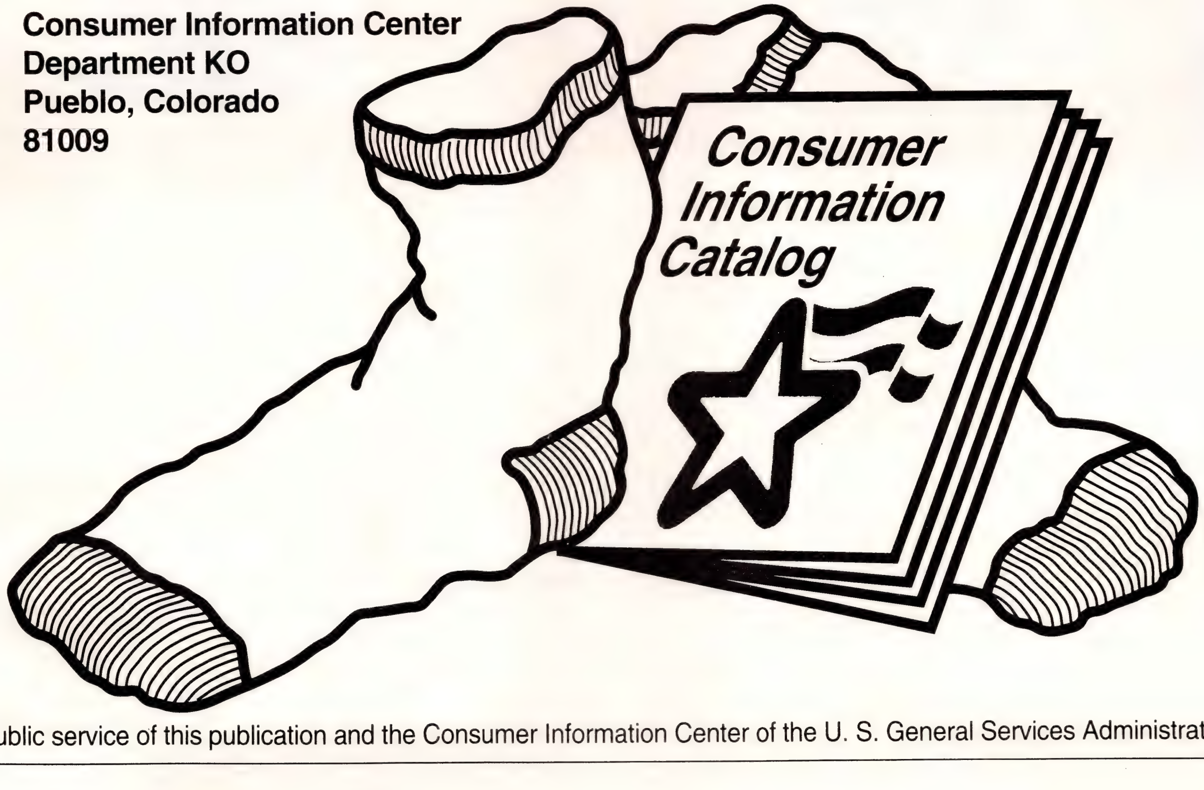

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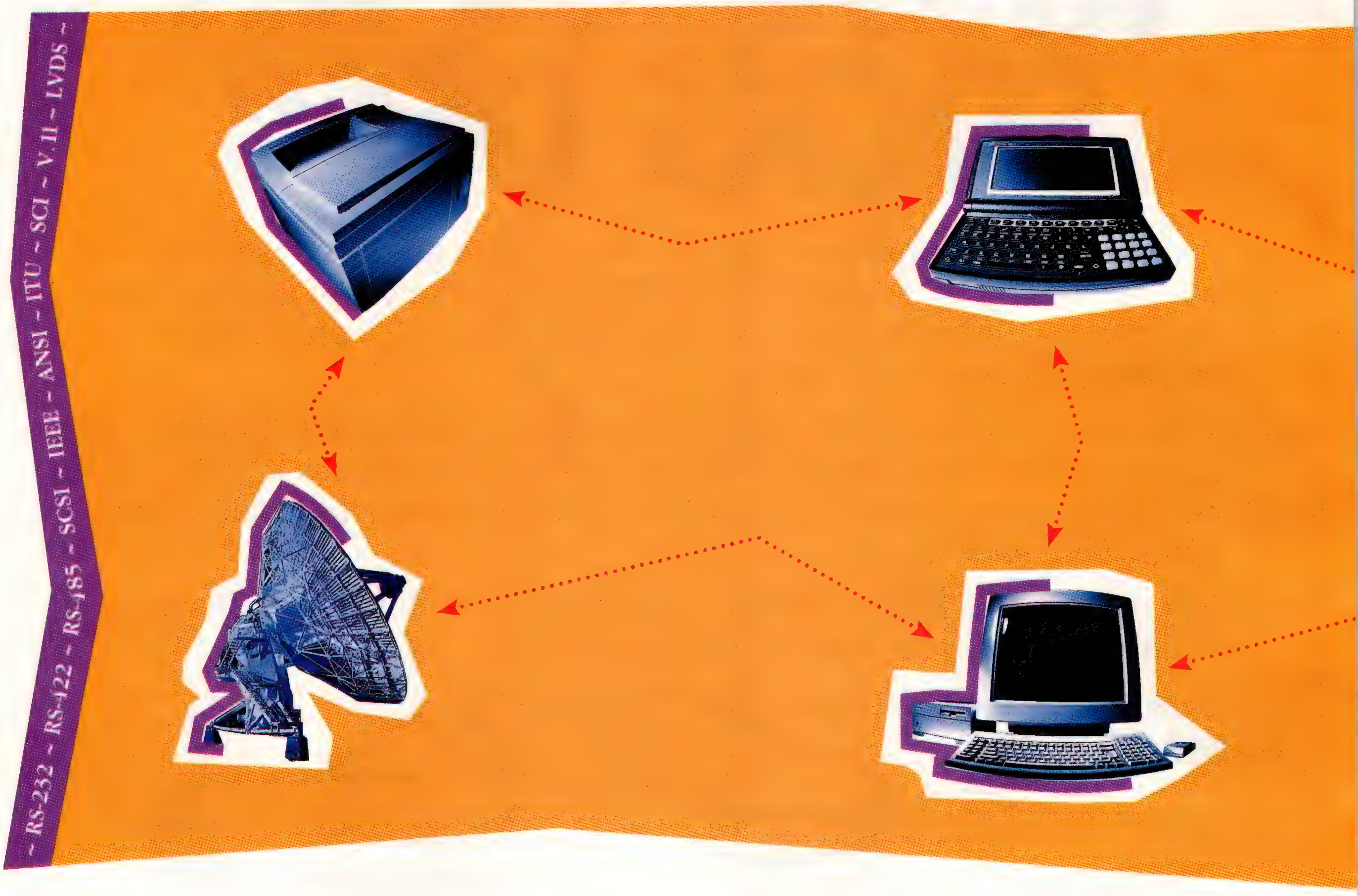
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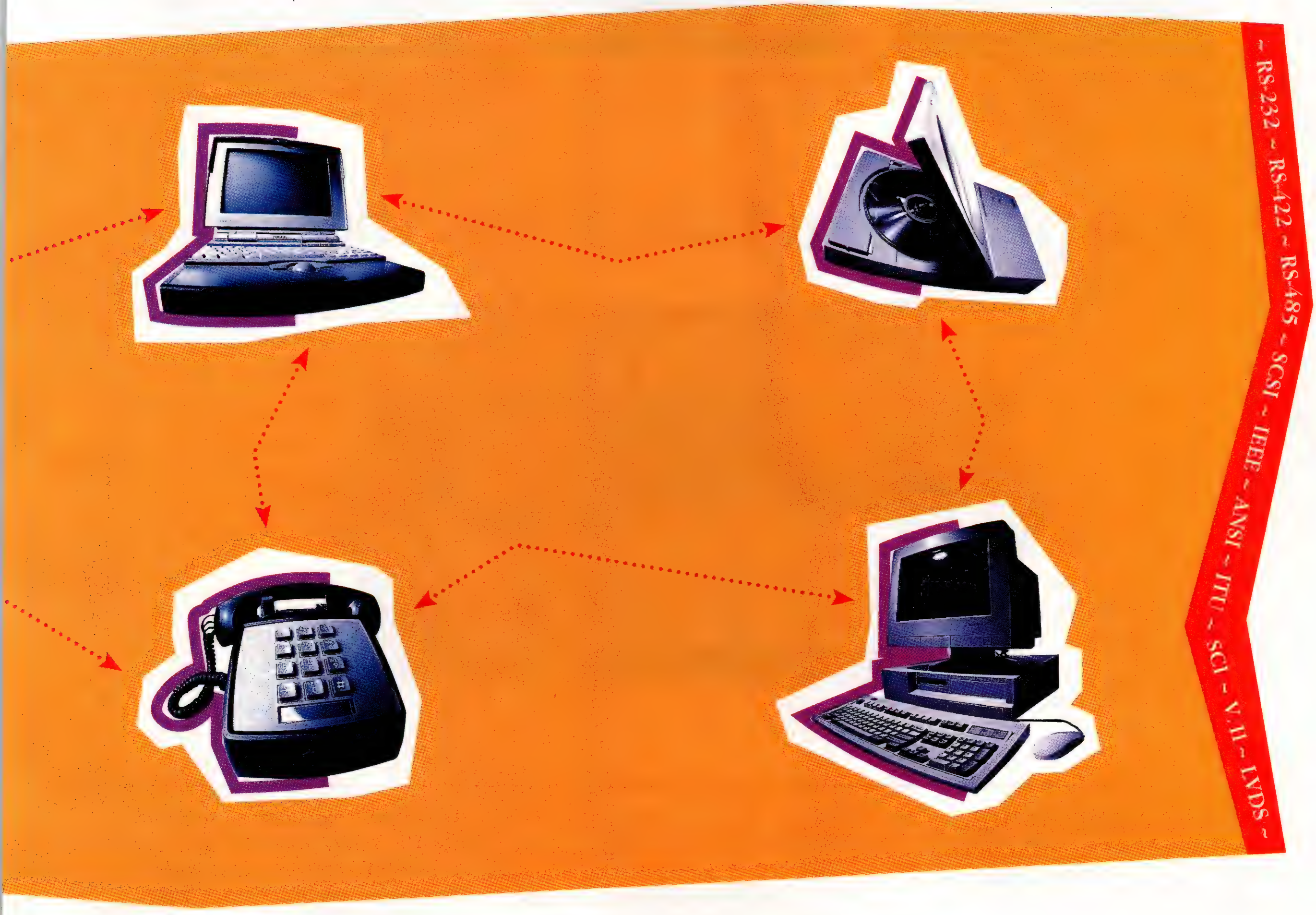
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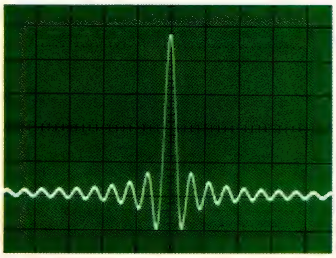

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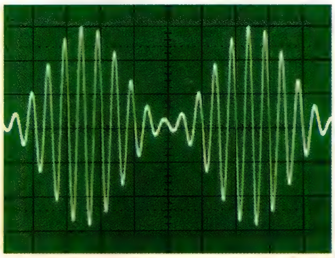

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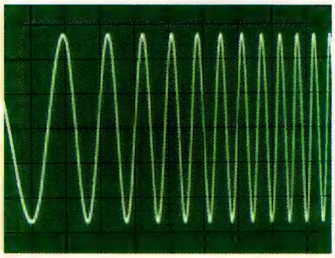

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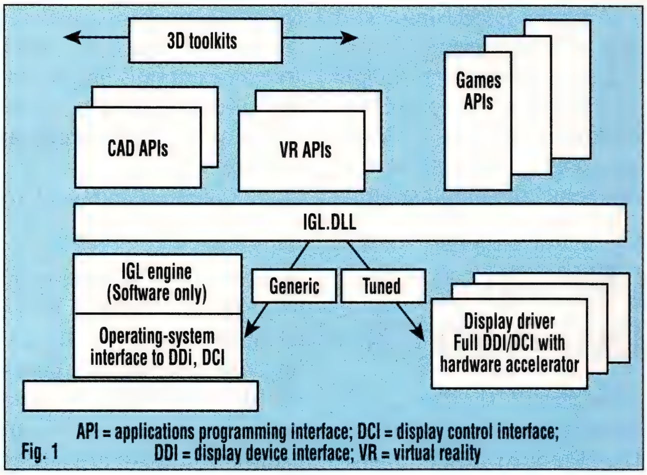
SOFTWARE STANDARDS PROMOTE FASTER GRAPHICS AND BETTER DISPLAY-DEVICE ACCESS

Though the Microsoft Windows interface is ideal for viewing data and making it easier to use applications, many graphics-oriented application developers (especially game developers) have shunned it. That's because Windows overheads make the graphics run slower than if the application were written under DOS. However, software designers at Intel Corp., Santa Clara, Calif., have crafted a new 3D graphics library that should attract those developers. Now, by using the library, DOS-like graphics performance under the Windows operating system can be achieved.

Graphics libraries aren't a new idea. They've been used by a number of companies, most notably Silicon Graphics Inc., Mountain View, Calif. Silicon Graphics has now opened its 3D library and made it a popular standard for workstation graphics—OpenGL. But in the PC world, there hasn't been a well-accepted standard for doing high-performance 2D or 3D graphics. Intel hopes to change that with its release of the Intel Graphics Library (IGL) later this year *(Fig. 1)*.


3D toolkits
CAD APIs
VR APIs
Games APIs
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IGL engine (Software only)
Operating-system interface to DDi, DCI
Generic
Tuned
Display driver Full DDI/DCI with hardware accelerator

Fig. 1 API = applications programming interface; DCI = display control interface; DDI = display device interface; VR = virtual reality

The IGL interface will define a mechanism to accelerate 3D drawing, while the display control interface (DCI) will help accelerate video playback. Together, the two standards promise to make the next-generation platforms true multimedia-capable machines. Details on IGL are sketchy at present, but it's known that it will deliver approximately a four-fold improvement over current Windows-based graphics performance when coupled with the DCI standard discussed later. An additional doubling of performance is possible by incorporating hardware acceleration.

IGL does provide device-independent access to 3D acceleration hardware, and with a tuned software port, will greatly increase rendering speed. Furthermore, in non-accelerated situations, it offers transparent emulation with some performance improvement over existing 3D software solutions.

In a related development involving Windows, Intel and Microsoft Corp., Redmond, Wash., last month unveiled the DCI, a device-independent, driver-level software interface *(Fig. 2)*. DCI provides access to display devices while maintaining compatibility with the Windows graphics-device interface (GDI). Such an interface may become an industry-wide agreement that could lead to a "standard" software interface for applications and display devices. Many companies with desktop and portable computers have needed such a standard to play back real-time video.

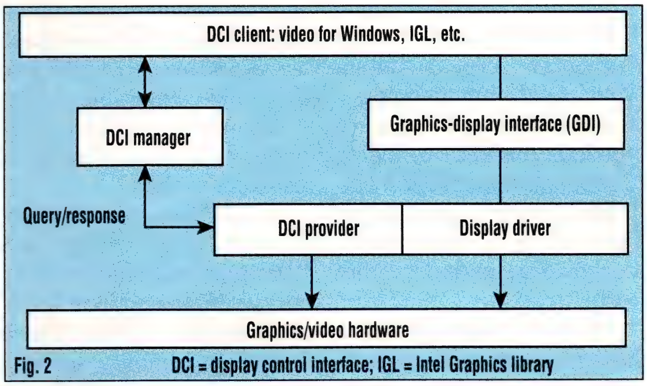

Fig. 2 DCI = display control interface; IGL = Intel Graphics library

The 1.0 release of DCI provides a device-independent method for Windows subsystem software, including the upcoming release of the Windows Chicago operating system (likely to be named Windows 4.0), to access display-device-independent features. This subsystem software includes 3D graphics packages, games interface packages, and digital video codecs. In the case of digital-video codecs, additional support in the standard allows any codec that already supports the DecompressEx message (as specified by the Video for Windows installable codec interface) to automatically take advantage of DCI capabilities.

DCI delivers improved video-playback quality when accessing YUV color formats, improved graphics and video quality when accessing image-stretching hardware, and support for double-buffered graphics. It also allows simultaneous access to standard and enhanced display device memory areas, provides smooth rendering of 3D graphics, and offers graphics overlays on video in a window. The interface doesn't offer access to software running on coprocessors that require display capabilities. Those designs typically have hardware-specific interfaces from the coprocessor to the display.

For now, DCI also will not function with Windows NT because DCI relies on the ability to directly access and draw on display memory. However, in Windows NT, display memory isn't exposed in the same way since it's accessible through Windows 3.1 or Chicago. Future releases of DCI may overcome the incompatibility with Windows NT.

Copies of the DCI specification are now available and can be obtained from either Microsoft or Intel through Internet at dci-ihv@microsoft.com or dci-ihv@ibeam.intel.com. First versions of the IGL specification will be available next month from Intel. The specification can be requested through Internet at 3Dgraphics@gomez.intel.com, or call David Schuler at (503) 681-8080.

LIQUID COOLING COAXES 30 W OF POWER FROM PLASTIC IC PACKAGE IN STILL AIR

Anticipating even more power-hungry chips than Intel's Pentium microprocessor, two packaging houses joined forces to successfully dissipate 30 W of power from a low-cost plastic IC package with natural convection (no forced airflow). This technology breakthrough, dissipating about three times what was possible previously, was achieved through a marriage of a state-of-the-art plastic package and liquid-based cooling techniques.

By cooling the PowerQuad package, developed by Amkor Electronics Inc., Chandler, Ariz., with the Oasis liquid-cooling technology developed by Aavid Engineering Inc., Laconia, N.H., engineers in Amkor's laboratories successfully used power levels of 25, 36, and 40 W. A prototype of the PowerQuad/Oasis system was shown at February's Semi-Therm Conference in San Jose, Calif. It achieved a steady-state power level of 25 W with junction temperatures maintained below 115°C. This starkly contrasts with the power level of 6 to 10 W attainable with forced-air cooling.

Another demonstration, this at 30 W, was performed at the 6th International TAB and Advanced Packaging Conference in San Jose in mid-February. Then a refined, production-ready version was unveiled at the Nepcon West show in Anaheim, Calif., in early March.

The low-cost PowerQuad2 plastic package used by Amkor for the PowerQuad/Oasis system is a 304-lead, 40-by-40-mm package with a built-in 32-by-32-mm heat sink/spreader made of solid copper. The package is mated to the Oasis cooling system using 3M Corp.'s thermally conductive tape. The IC used in the demonstration is a small Delco thermal test chip.

The PowerQuad2 package is attached directly to the large copper heat spreader. This direct connection results in a very low junction-to-case thermal resistance, typically about 0.3°C/W.

Amkor Electronics and Aavid Engineering plan to jointly characterize Amkor Eelctrtonics' various PowerQuad2 packages with Oasis cooling systems. Aavid will be developing optimized designs of standard heat exchangers/condenser systems for use with the entire PowerQuad family of packages, which spans 44 to 304 leads.

Aavid developed the Oasis system to solve the extreme thermal problems facing designers who plan to use next-generation microprocessors. The passive liquid-cooling system provides noiseless operation, consumes no power, and has no moving parts, such as pumps or fans, to wear out. The system uses 3M's Fluorinert cooling fluid, which is inert, non-toxic, non-flammable, and non-ozone-depleting. For more information on the PowerQuad2 IC packages, contact Amkor at (602) 821-5000. For more details on the Oasis liquid-cooling system, call Aavid Engineering at (603) 528-3400.

DAVID MALINIAK

PROFILES ALLOW FIBRE CHANNEL STANDARDS TO EXPAND BY NARROWING APPLICATION FOCUS

The complex standard covering the Fibre Channel interface includes many features and functions that some systems needn't implement to remain compatible with the standard. By focusing on specific applications of Fibre Channel, members of the Fibre Channel Systems Initiative (FCSI), headquartered at Sun Microsystems Computer Corp., Mountain View, Calif., are defining a series of "profiles." These are vertical market segments that use a subset of the entire Fibre Channel specification, thus reducing implementation overheads and system costs.

The first profile, released last year, created a subset of the Fibre Channel standard optimized for a serial version of the Small Computer Systems Interface (SCSI). In addition to the profile, the FCSI organization also formalized the procedure to create additional profiles—the Fibre Channel profile structure. Along with the procedure for creating profiles, the FCSI group defined a common feature set profile—a base set of features that all Fibre Channel-compatible systems must include to provide a minimum degree of interoperability.

A profile can be perceived as a vertical slice through the standard with all significant options specified *(see the figure)*. Those options include service, logical, and physical parameters. A total of 19 optional ways are available in the standard just to implement a connection (fiber optics, copper twisted pairs, coax, etc.), and many options exist at the link level as well.

In Fibre Channel, there are both symmetrical and asymmetrical profiles. For a peer-to-peer system such as the transmission control protocol/internet protocol (TCP/IP), the profiles are symmetrical. But in a host/peripheral system like SCSI or IPI-3, the profiles are different because each end performs different functions.

The latest standard profile, unveiled last month at the IEEE Compcon Conference in San Francisco, Calif., defines a subset that makes it possible to employ TCP/IP over optical Fibre Channel interfaces. By using the profile, designers can develop TCP/IP-based products that will be interoperable with any other Fibre Channel products. The high bandwidth of Fibre Channel systems provides users with transfer rates in excess of 1 Gbit/s.

For the TCP/IP profile, several options in the Fibre Channel standard were included as standard features, thus tuning the subset for communications, explains Peter Walford, a principal at Plexippus Consulting Inc., Palo Alto, Calif. For instance, Sequence Streaming, an option in the overall standard, is now part of the TCP/IP profile. This feature eliminates latencies that could occur when a node is waiting for acknowledgements.

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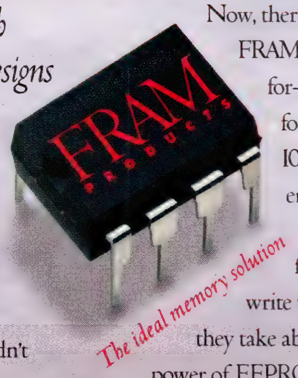

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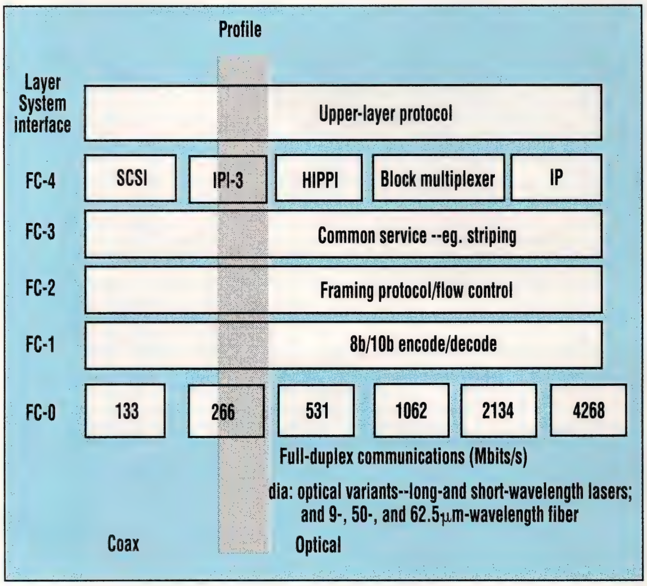
Furthermore, the profile defines a maximum transmission unit size of 64 kbytes (more specifically, 65,280 bytes including headers, and 248 bytes for expansion); in contrast, the sequence size for typical Internet transfers is 532 bytes (non-TCP/IP mode).

In addition, the new profile includes as part of its definition the address resolution capability, which allows nodes on Fibre Channel to locate and identify each other. The base standard defines the need for such a capability, but doesn't define how to implement the address resolution. The profile includes the next level of definition as well as guidelines to implement address resolution.

Such a high bandwidth, according to Ed Frymoyer, the program manager for FCSI and a product manager at Hewlett-Packard Co., Cupertino, Calif., will allow clustered solutions to operate more like a single integrated, high-performance parallel-processing system. In addition, Fibre Channel supports switched connections with over 16 million addresses in its fabric. That gives users an almost unlimited number of available nodes. With the large address space, high-bandwidth point-to-point connectivity, and switched-I/O functionality, Fibre Channel provides an infrastructure that can enable new classes of clustered solutions.

By having a common profile to implement TCP/IP over Fibre Channel, designers will be able to develop more cost-effective implementations than if the full Fibre Channel standard were used. The profiles eliminate much of the overhead that wouldn't typically be used for TCP/IP interfaces. That, in turn, simplifies the system implementation and reduces both the time to market and the cost to implement the interface.


Profile
Layer System interface
Upper-layer protocol
FC-4
SCSI
IPI-3
HIPPI
Block multiplexer
IP
FC-3
Common service --eg. striping
FC-2
Framing protocol/flow control
FC-1
8b/10b encode/decode
FC-0
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266
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1062
2134
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The combination of the TCP/IP profile and the previously-released SCSI profile gives designers a strong start in developing an interoperable system based on standards. Because many networks already use TCP/IP, the Fibre Channel TCP/IP profile gives designers a blueprint that enables network users to take advantage of the moderate cost, the high-performance, the scalability, and other benefits of Fibre Channel.

Furthermore, Fibre Channel supports both channel and network traffic traveling over a single medium and single hardware connection. As a result, it provides the first solution that allows both storage and network data to run simultaneously.

The Fibre Channel profiles are now available electronically via anonymous ftp on Internet from playground.sun.com, directory /pub/incoming; or by sending a request for a hard copy to FCSI Administration, c/o Gladys Van Polanen Petel, Sun Microsystems, Mailstop UMTV 16-10, 2550 Garcia Ave., Mountain View, Calif., 94043-1100. Or call Peter Walford at (415) 508-8354.

DAVE BURSKY

PROTOTYPE E-MAIL SYSTEM INCLUDES MULTIMEDIA, INTELLIGENT RETRIEVAL

Once a toy for hardcore computer hackers and technophiles, e-mail is now considered by many to be a business tool that's as indispensable as the telephone. Though the telephone allows people to communicate independent of distance, electronic messaging permits individuals to exchange information and work collaboratively, regardless of their location or schedules. A recently unveiled prototype e-mail system will add a new dimension to this capability by making it possible for users to exchange interactive, multimedia messages containing voice, text, video, and graphics.

Developed at the Siemens Corporate Research Center, Princeton, N.J., the Siemens multimedia mail system (SMMS) gives users the ability to attach any type of video, audio, or binary file onto a conventional e-mail message. In addition, SMMS permits users to search and retrieve files from its archival system with a variety of sophisticated tools, including non-specific, content-based searches and a unique "video browsing" feature.

The advanced features of SMMS will rapidly lend themselves to graphics/video-intensive applications, such as movie and video production, medical archives, and newspapers. Dr. Arding Hsu, group leader of Siemens image and video management group, noted that the new video-browsing technology allows for much faster access and review of material than conventional fast-forward/rewind techniques.

The video browser can send live messages or clips to others as a part of the e-mail system. With proper processing, just three minutes of selected video can provide a fairly complete version of an hour-long clip. Explains Dr. Hsu, "By operating directly on compressed video information, the computer algorithm divides the material into meaningful segments and automatically selects one representative frame from each scene. Thus, a two- or three-hour video clip can be viewed in about five minutes with no loss of continuity." He says that a patent is pending on the browser.

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	4 Meg	x4	70, 80	Now
		x16	60, 70, 80	3Q94/4Q94
Synchronous DRAMs	16 Meg	x8	10, 12, 13	3Q94/4Q94
DRAM Modules	32MB	x32, x64, x72	60, 70	3Q94/4Q94
	16MB	x32, x64, x72	60, 70	3Q94/4Q94
	8MB	x32, x64, x72	60, 70, 80	Now
	4MB	x32	60, 70, 80	Now
88-Pin DRAM Cards and MiniCards	32MB	x32	60, 70	3Q94/4Q94
	16MB	x32	60, 70	3Q94/4Q94
	8MB	x32	70, 80	Now
	4MB	x32	70, 80	Now
SRAMs	4 Meg	x4, x8, x16	12, 15, 20, 25	3Q94/4Q94
	1Meg (revolutionary)	x4, x8, x16	15, 20, 25	Now/3Q94
	1Meg (evolutionary)	x1, x4, x8	15, 20, 25	Now
	256K	x1, x4, x8	12, 15, 20, 25	Now
Synchronous SRAMs	1 Meg	x18, x36	7, 10, 12, 15, 17	Now/3Q94
SRAM Modules	4MB	x32	15, 20, 25	4Q94/1Q95
	1MB	x32	20, 25	3Q94/4Q94
	512KB	x32	20, 25	3Q94/4Q94
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The SMMS e-mail system also features dynamic annotation and image retrieval. Dynamic annotation means that an attached image, video frame, or video clip can be annotated with voice, graphics markings, or mouse gestures. The content-based search function will assist in archival searches. It comes in handy when written descriptions, posed as a computer queries, aren't possible because of insufficient keyword classification.

Content-based image retrieval provides users with the power of associative searches through a large image archive by giving the computer a rough sketch or image fragment and telling it to look for "something like this." Currently, images stored in SMMS must be identified and manually classified before searches can be performed. Eventually, notes Hsu, the system will be able to search for and retrieve drawings that haven't been catalogued.

While this represents the ultimate goal, he cautions that it may be as long as five years before a fully-developed system is available for general use. Once on the market, this retrieval method may open up many areas to computerized image archiving that previously couldn't be considered due to the volume and ambiguity of the images. At this point, three or four working systems are expected to be in use by Siemens operating companies by the end of the year.

The imaging department is currently conducting research in the areas of image database management, image analysis, and imaging hardware and architecture. Image-processing algorithms are being developed for applications in medical diagnosis and treatment, industrial automation, and safety systems. For more information about the SMMS retrieval system, contact Dr. Hsu at the Siemens Research Center at (609) 734-6548.

LEE GOLDBERG

"NOSE-ON-A-CHIP" SENSOR COULD GIVE COMPUTERS THE ABILITY TO SMELL

Through the use of various transducers, computers can emulate the human senses of sight, hearing, and touch. However, one human sensory capability that continues to elude engineers is the sense of smell.

To that end, scientists at IBM Research Division's laboratories in Zurich, Switzerland recently developed what's claimed to be the world's most sensitive heat-sensing instrument. When specially configured, this instrument could be the key to emulation of the olfactory organ.

The instrument, called a calorimeter, is a thousand times more sensitive than any similar instrument available today. It can measure the heat generated in chemical reactions with a resolution as small as 1×10^{-5} °C. The instrument's sensitivity limit is estimated at about 1 pJ.

The heat-sensing technique involves the use of a micromechanical silicon lever that's coated with aluminum. When heated, the miniature silicon lever bends because of the different coefficients of thermal expansion between the aluminum and silicon materials. The amount of bending of the lever directly indicates how much heat was absorbed by the lever. IBM's researchers used a laser to measure the the extremely small amount of bending, which can be as little as 1/100th the diameter of an atom.

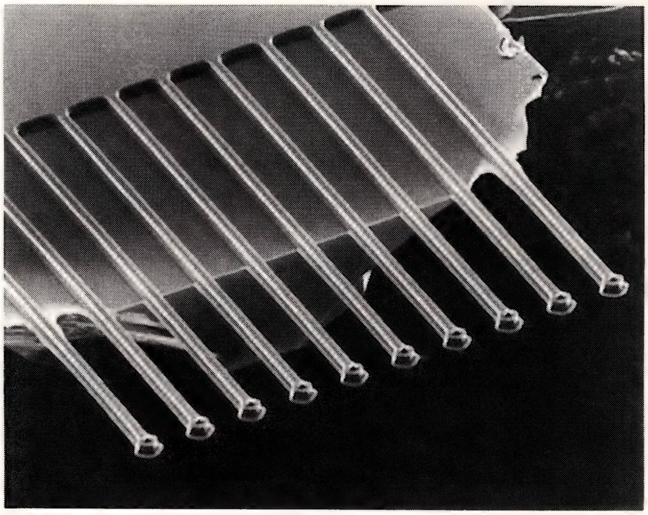
In one demonstration, a thin layer of platinum material was applied to the aluminum-coated silicon lever. The platinum material, in the presence of a mixture of oxygen and hydrogen, functioned as a catalyst that promoted the combining of the gases to form water. In the process, the platinum layer generated heat that was absorbed by the lever, causing it to bend. By carefully monitoring and measuring that bend, IBM's researchers were able to show that hydrogen and oxygen do not combine at a uniform rate. The rate actually oscillates with time, a phenomenon that was known to occur but had never before been sensed with a calorimeter.

The concept of a "nose on a chip" comes in when one considers the size of the lever, which is microfabricated with IC technology. The lever is about 1.5-µm thick and 400-µm long *(see the photo)*. Given such extremely tiny dimensions, conceivably, arrays of hundreds of levers could be integrated on a single integrated circuit.

If each lever were to be coated and thereby sensitized to detect a specific chemical, the resulting combination would function as a powerful olfactory sensor. Even coatings such as reaction-specific enzymes and bacteria could be used. Moreover, because the calorimeter is so sensitive, chemical reactions involving only a few molecules could be detected.

Typically, ordinary individuals can discern from among hundreds of odors. Trained experts have been known to recognize several thousand. But IBM's researchers believe that the apparatus for this technique could be incorporated into a portable package with a PC, providing an instrument capable of detecting almost any gases and pollutants.

DAVID MALINIAK



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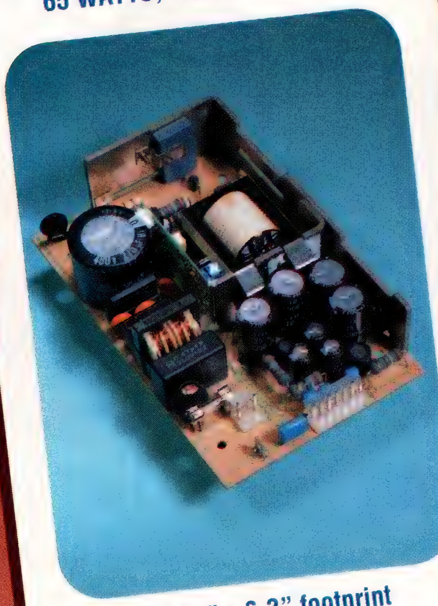
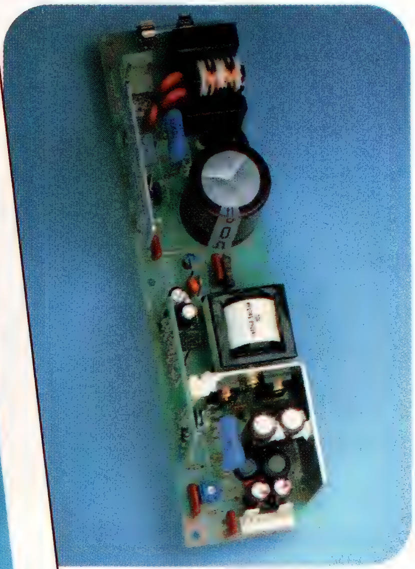


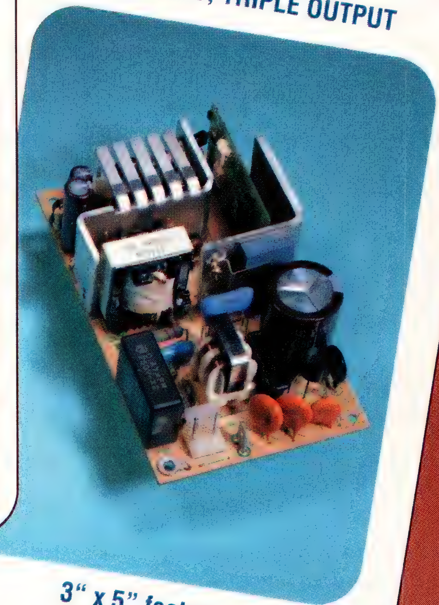
3.94" x 6.3" footprint
100 x 160mm

MODEL MRW 145KV
28 WATTS, DUAL OUTPUT



2" x 8" footprint
50 x 200 mm

MODEL KRW 352KV
40 WATTS, TRIPLE OUTPUT



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SHARP

PROGRESS REPORT

Dedicated to the proposition that one good idea leads to another.

From early light to the latest

No matter how automated, computerized and roboticized tomorrow's production line becomes, its intelligence must be supported by the systems to receive and transmit information and to protect and coordinate its motor skills.

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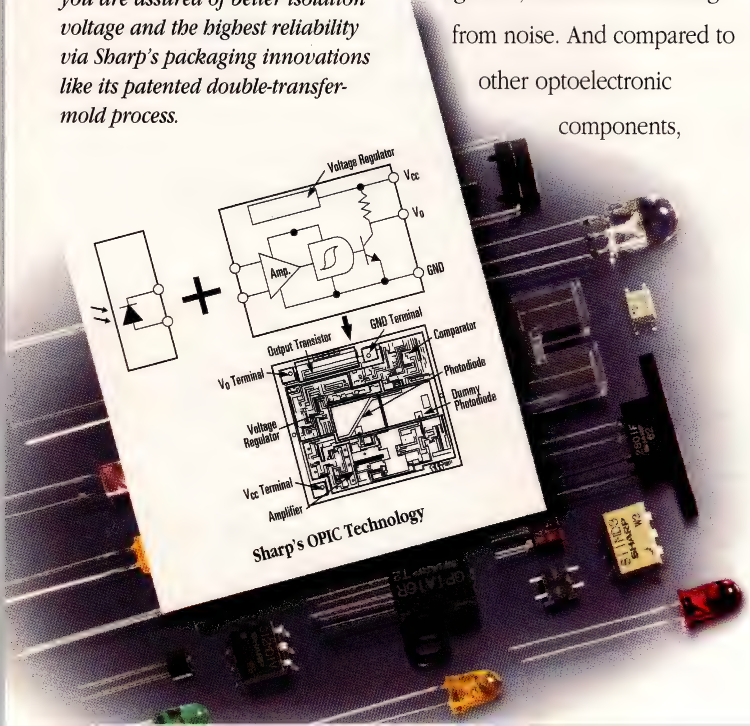
**RELIABILITY.
CAPABILITY.
AND CHOICE.**

One faulty photocoupler can be the weak link that paralyzes a production line. Your best hedge against this is the added voltage isolation protection afforded by Sharp's patented double-transfer-mold technology. Sharp uses two separate molds of epoxy resin as part of a process that promises higher isolation voltage, tighter tolerances and more reliable performance even as the size of photocouplers keeps shrinking.

And when it comes to putting the most opto capability on the least real estate, you can turn to Sharp's Optical Integrated Circuit (OPIC) technology. We offer more than 50 ways to

With three decades of opto technology behind it, Sharp has pushed device functionality to new extremes. Sharp's proprietary Optical IC (OPIC) process technology combines photodiodes and their peripheral circuitry on a single chip to achieve new dimensions in device miniaturization. In addition, you are assured of better isolation voltage and the highest reliability via Sharp's packaging innovations like its patented double-transfer-mold process.



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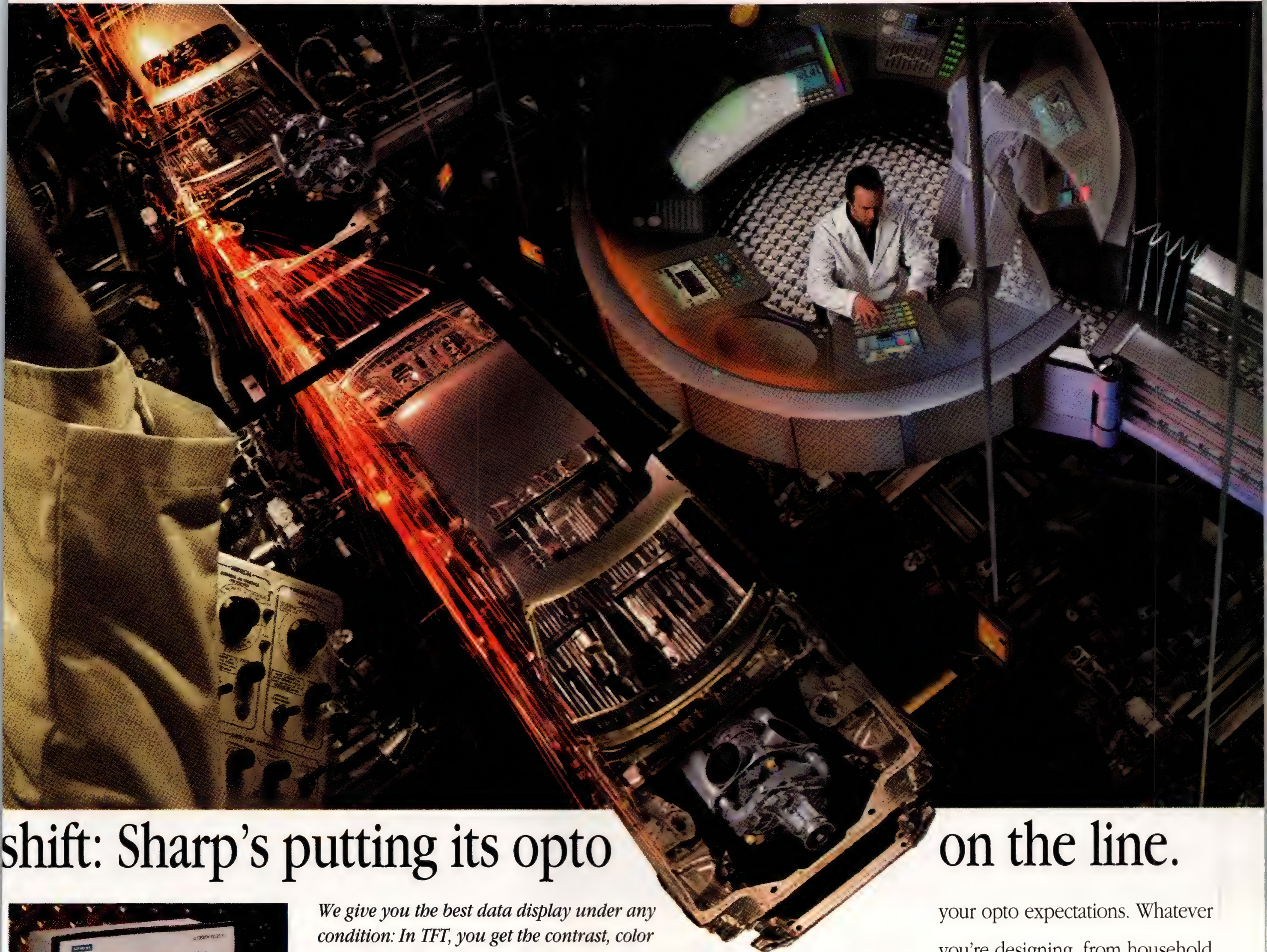

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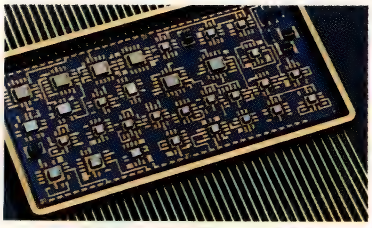

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COVER FEATURE

A 50-KGATE MODULE, WHICH COMBINES SRAM-BASED CPLDS, MCM TECHNOLOGY, AND A PROGRAMMABLE INTERCONNECTION CHIP, EASES ASIC EMULATION.

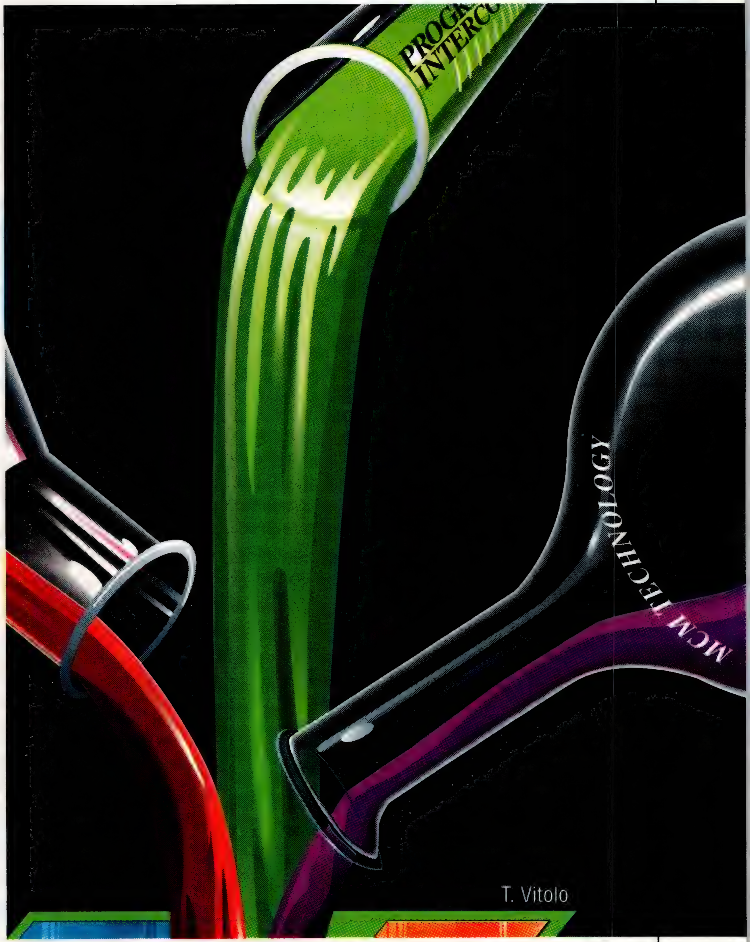
CPLD MODULE PACKS 50K USABLE GATES, 360 I/O PINS

DAVE BURSKY

Patience can become quite a valued commodity in the design of increasingly complex systems. When software simulations are used to verify a design, just a few microseconds of execution often translates into hours or days of simulation time. Moreover, some functions—such as graphics control—need close to real-time throughput to prove that they work.

One approach that has proven feasible but expensive is the use of large arrays of static-RAM-based, field-programmable gate arrays to form hardware emulators. Such emulators have prices starting at about $50,000 for a small system containing between 10 and 20 kgates. Larger systems carry considerably larger price tags. In these systems, the FPGAs are arranged on large boards that have a fixed interconnection pattern between the FPGAs. These boards then are downloaded with the desired configuration patterns, and multiple boards or systems can be used to simulate one or more complex custom chips. Such emulation systems can run many times faster than the software-only approach, but are speed-limited to a fraction of expected throughput due to the long interconnections across multiple boards.

However, the complexity of the ASIC that can be simulated/emulated is limited by two key factors—FPGA complexity and the rigid interconnections between the FPGAs. Designers at Altera addressed both of those issues and came up with a close-to-ideal emulation solution: They created a high-density, programmable, lower-cost system that can be used without lots of overheads or the need for emulation experts.



T. Vitolo

Their approach involves three different technologies: a multichip module, SRAM-based complex programmable-logic-device (CPLD) chips, and an SRAM-based field-programmable interconnection chip (FPIC). The MCM combines four of the highest-density SRAM-based CPLD chips currently offered by Altera with the SRAM-based FPIC unveiled by Aptix Inc., San Jose, Calif., about one year ago. The combination of those three technologies yields the highest-gate-count, programmable-logic circuit to-date—a

50,000-usable-gate MCM at a cost of less than a tenth that of previous emulation systems. Because it's SRAM-based, the MCM's logic can be reconfigured in the field to emulate just about any digital circuit.

Furthermore, according to numerous market studies, about 70% of all ASIC designs contain less than 50,000 gates. That means that the MCM can tackle about 70% of all circuit emulations. And, the same version of Altera's fitter and partitioning software, enhanced with the Aptix interconnection and routing software, provides designers with the software needed to map their designs to the MCM.

Each of the four CPLDs mounted in the MCM is an EPF81188. It's the largest member of Altera's Flex 8000 family, packing about 24,000 raw gates and 1168 registers (the 1168 total is slightly lower than the actual register count on the EPF81188 since a few registers are used for the internal MCM connections). As a result, the total gate and register count puts the MCM density at a level about two years ahead of what can be achieved monolithically, giving designers a head start.

All four CPLDs are tied together through the MCM's 32-layer ceramic substrate to a lone Aptix FPIC. The FPIC provides 1024 connection points that allow signals to be routed from any I/O line on one CPLD to one or many other I/O lines within the MCM or to the outside world *(Fig. 1a).* The FPIC used in the MCM is actually Aptix's second-generation interconnect chip, which will be described in detail at next month's IEEE Custom Integrated Circuits Conference in San Diego, Calif. Enhancements made in the FPIC architecture improve signal routability and shorten the development time.

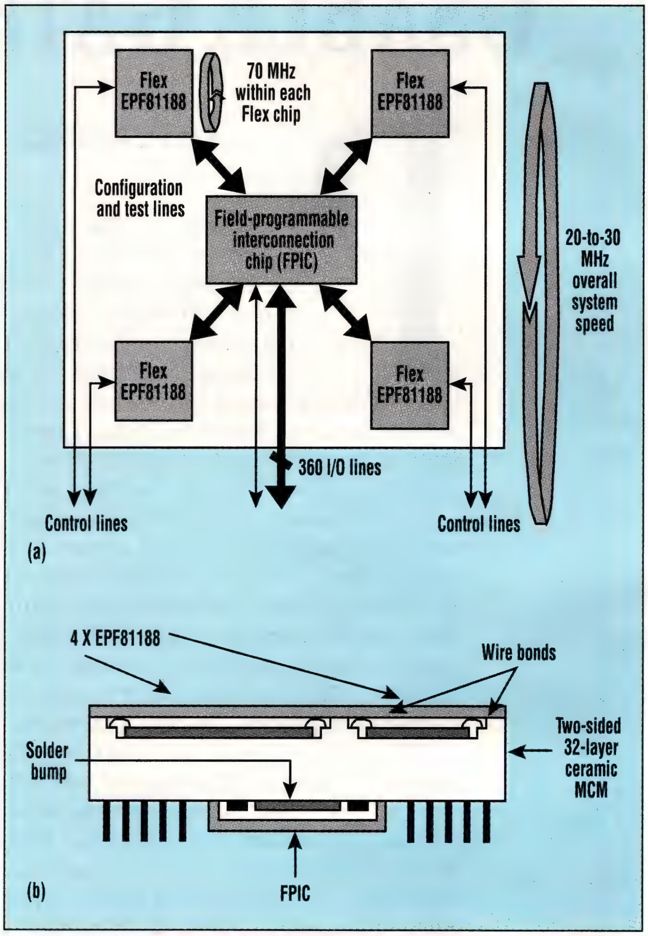
Functions that can be partitioned to operate within one of the four CPLDs will operate at clock speeds of about 70 MHz. The additional delays of going from chip to chip limit the overall operating speed of the four-chip MCM to only between 20 and 30 MHz. That "only" is a misleading term, however. Although it's low versus what can be achieved by direct silicon implementation, it's thousands of times faster than what could be achieved using a software simulation of a target design. Such speeds should adequately represent how well the target circuit implements a desired function.

The Flex architecture incorporates a large matrix of logic elements (LEs), each of which contains a four-input lookup table for combinatorial logic and a programmable register for sequential logic. Each LE also includes dedicated carry and cascade chains to increase the speed of counters, adders, and wide fan-in functions. The LEs are grouped into sets of eight to create logic array blocks (LABs). Each LAB has dedicated internal but programmable interconnections, and also connects to more hierarchical-routing levels.

The EPF81188 contains 126 LABs arranged in six rows and 21 columns. Interconnections between the LABs is provided by the FastTrack interconnects—a series of continuous lines that run the entire length and width of the chip. Bidirectional I/O elements, which include flip-flops and three-state buffers, are located at the end of each row and column of all FastTrack interconnect structures.

Although ASIC prototyping probably will be the most popular application for the EPF8050M, it won't be the only one. Even though the single-unit price for the MCM is $3995 per module, there are many value-added applications (such as in imaging and programmable hardware) in which the value is in the algorithm rather than the hardware. By allowing each algorithm to optimize the underlying hardware, thus improving the efficiency of each algorithm, higher-performance subsystems can be implemented without pushing clock speeds past silicon limits.

All of the CPLDs' I/O lines are routed through the FPIC to reach the outside world. A total of 360 I/O lines are available on the 516-lead pin-grid-array package. Those pins are set up on staggered-pitch 70-mil centers to minimize the board area


Flex EPF81188
70 MHz within each Flex chip
Flex EPF81188
Configuration and test lines
Field-programmable interconnection chip (FPIC)
20-to-30 MHz overall system speed
Flex EPF81188
Flex EPF81188
360 I/O lines
Control lines
Control lines
(a)
4 X EPF81188
Wire bonds
Solder bump
Two-sided 32-layer ceramic MCM
(b)
FPIC

1. FOUR 25,000-GATE CPLDs and a programmable-interconnection chip are melded together on Altera's EPF8050M, which packs a total of 50,000 usable gates. The chip delivers three times the gate count of any commercially available monolithic high-capacity programmable-logic device. Logic implemented within one of the Flex chips can operate at clock speeds up to 70 MHz, while circuits that extend across the entire MCM can operate at 20 to 30 MHz (a). The four Flex chips are first housed in ball-grid-array packages, and the four BGAs are then mounted on the top side of the MCM package. Wiring in the 32-layer ceramic substrate routes the signals between the Flex chips and the outside world through the field-programmable interconnection chip mounted on the bottom of the package with solder bumps (b).

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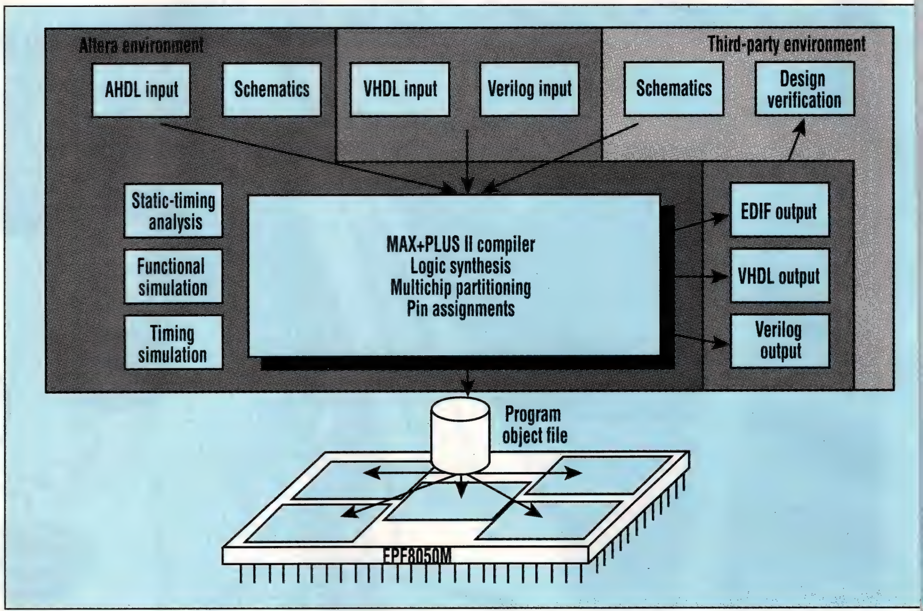

2. A FULL SUITE OF DESIGN TOOLS in the MAX+PLUS II software helps designers in capture, partition, and place and route their designs on the 50,000-gate multichip CPLD. Designs can be entered using schematics or hardware-design languages and various analysis tools—static-timing analysis, functional simulation, and timing simulation. A design can be verified before a file is created to configure the arrays.

consumed by the package, which measures just over two inches on a side. To squeeze the four chips and the programmable interconnect chip into the 2-in. square area of the package, Altera's designers first housed the CPLDs in ball-grid-array packages. Then they mounted the BGA packages on the top side of the MCM, while the FPIC chip was mounted on the underside of the package located in the center of the array of pins *(Fig. 1b)*.

Control lines that allow the host system to download the configuration pattern also are brought out. However, rather than daisy-chain the four CPLDs and the FPIC, each chip has its own set of control and data lines routed to the package pins. That makes it possible for each chip to be individually tested to ensure functionality before the configuration pattern is loaded. Each Flex chip requires a total of 192 kbits of configuration data, while the FPIC needs just 52 kbits. Consequently, a 1-Mbit EPROM or flash memory could hold all of the configuration data, or the host system can download the data from disk.

Programming the EPF8050M is almost as straightforward as developing the configuration pattern for a board with several CPLDs. The MAX+PLUS II software for IBM and compatible PCs or Unix workstations handles everything from design capture to placement and routing. Designs can be entered with either schematic or hardware-design-language (AHDL, VHDL, Verilog HDL) descriptions *(Fig. 2)*. The compiler in Altera's MAX+PLUS II software automatically synthesizes and partitions the design into the four EPF81188s, and then generates a programming file for the CPLDs and the FPIC (with the addition of the Aptix configuration software). Designs can be verified using Altera-supplied simulators and timing analyzers, or output-timing-annotated EDIF, Verilog, or VHDL net lists that can be used with third-party CAE tools.☐

PRICE AND AVAILABILITY

The 516-pin EPF8050M multichip module sells for $3995. Samples will be available in the third quarter of this year.

Altera Corp., 2610 Orchard Pkwy., San Jose, CA 95134-2020; Cliff Tong, (408) 894-7000. **CIRCLE 512**

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MODERATELY	525
SLIGHTLY	526

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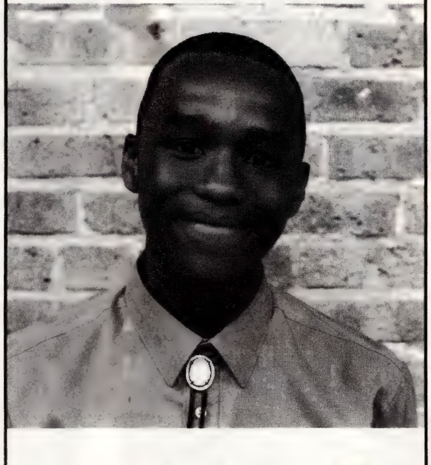

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Sure, you could crawl in a hole and hide. But wouldn't our bright spacious cabins be more comfortable?

Photo: Frank Moscati

Al Wallack, Sr. VP Marketing, Celebrity Cruises, after returning from having his hearing checked.

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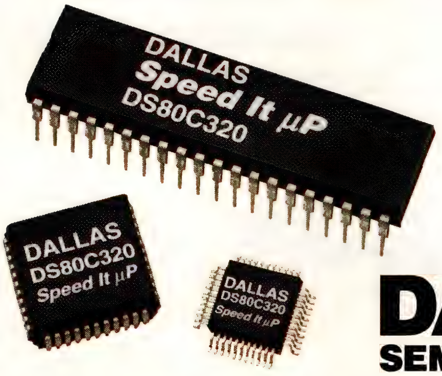

The DS80C320 performs three times faster than other 8051s at the same crystal speed. Running at 25 MHz, the DS80C320 can do six times as much work as a standard 8051.

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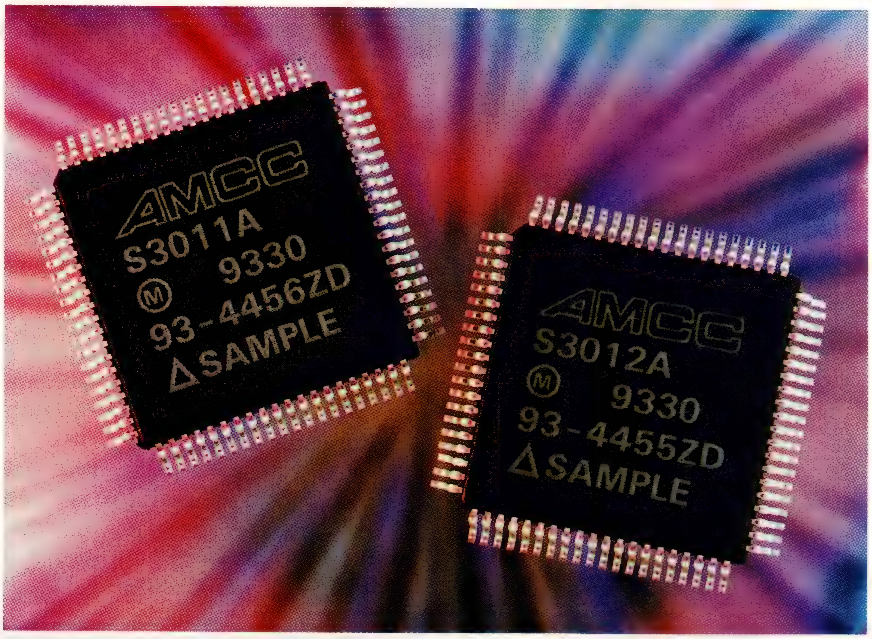

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ATM SILICON: READY FOR TAKEOFF

LEE GOLDBERG

ATM CHIPS CAN PUT YOUR PRODUCT IN THE DATA FAST LANE.

Asynchronous transfer-mode (ATM) communication is no longer simply a buzzword used by industry analysts and keynote speakers. With the first generation of working hardware being delivered, ATM is ready to compete for leadership in the emerging world of integrated networks. Many workstation vendors have announced plans to provide ATM-compatible products. In addition, many local- and wide-area-network (LAN and WAN) equipment suppliers have already introduced hubs, routers, and switches that support this high-speed data protocol.

Fueling the ATM revolution is the first generation of ATM interface chips. A number of top semiconductor IC manufacturers, such as Advanced Micro Devices, Fujitsu Microelectronics, Integrated Telecom Technologies, National Semiconductor, Standard Microsystems, and Texas Instruments have jumped on the ATM bandwagon with silicon devices *(see the table)*. Using them, engineers can rapidly design ATM-capable equipment that will mesh with both current and future networks. The ATM protocol implemented by these chip sets provides a seamless method for translating data between an ATM network, data-processing equipment, and other non-ATM-based networks.

The development of ATM communications applications is expanding rapidly. The technology can efficiently create high-speed, switched, variable-bandwidth, "virtual" channels within broadband networks. It can also transport many kinds of data (file transfers, voice, fax, video, etc.) over both optical-fiber and copper media.

Adding to the momentum, several companies have formed strategic alliances with equipment manufacturers to help establish their approach to ATM industry standards. For example, Texas Instruments teamed with Sun Microsystems to develop a chip set that forms the heart of an SBus-based ATM adapter board, thus turning any Sun workstation into an ATM-capable unit *(see "Board-level ATM solutions have arrived," p. 62)*. The complexity of ATM chips, the move toward shorter development cycles, seamless software/hardware interfaces, and the need to develop viable "plug-and-play" applications will mean we'll be seeing more such strategic alliances in the future.

Contributing to the rapid expansion and acceptance of ATM technology is the ATM Forum, a broad-based alliance of manufacturers and users that support and help develop the evolving ATM protocol. The ATM Forum seeks to maintain compatibility with existing systems, and establish interoperability standards between them.

To accelerate the process of standards creation and thus maximize user acceptance, the Forum has embraced existing data-communication standards (such as DS1/3 and the synchronous optical network/synchronous digital hierarchy, or Sonet/SDH) wherever possible. Manufacturers can build upon these existing transmission technologies by developing a consensus about standards selection and providing for their interoperability through ATM. This significantly reduces the development time and cost of early generation products.

FLEXIBLE AND EFFICIENT

ATM communications offers greater flexibility and efficiency than traditional LAN structures like Ethernet and token-ring networks because it's a switched and multiplexed technology. Whereas existing data-communications networks use shared-media-access techniques to grab a specific information stream from a broadcast signal, an ATM network employs a switched and multiplexed architecture that establishes a temporary, dedicated channel within the bandwidth of the transmission path. Once this "virtual" channel is established, data packets need only carry the name of the channel with them rather than explicit routing information. As a result, the amount of overhead required with conventional routing schemes is reduced quite dramatically.

Another distinctive trait of the ATM protocol is its fixed-size, 53-byte data cells. The small, uniform cell size permits multiplexing many data streams in a broadband channel

RESOURCES FOR DESIGN ENGINEERS

Key sources of information for engineers and managers involved with ATM technology:

THE ATM FORUM
303 Vintage Park Dr.
Foster City, CA 94404
Phone: (415) 578-6860
Fax: (415) 525-0182
E-mail: info@atmforum.com
This is *the* ATM resource. This group is the industry consortium that's facilitating the development of the ATM standards at all levels. If you use ATM in any way, you should get involved with the Forum. Their newsletter, "53 BYTES," is a great little publication that keeps you up-to-date on all areas of the ATM world. In addition, the Forum sponsors technical workshops on all aspects of ATM at conferences throughout the country. Membership also gives you access to technical publications and support.

ATM User Network Interface Specifications: Version 3.0
Author: The ATM Forum
Publisher: Prentice-Hall
Cost: $35
This book spells it all out for you, every aspect of every layer of the ATM protocol. While not light reading, the book is written in plain English, targeted at engineers who need good, solid data on putting ATM to work.

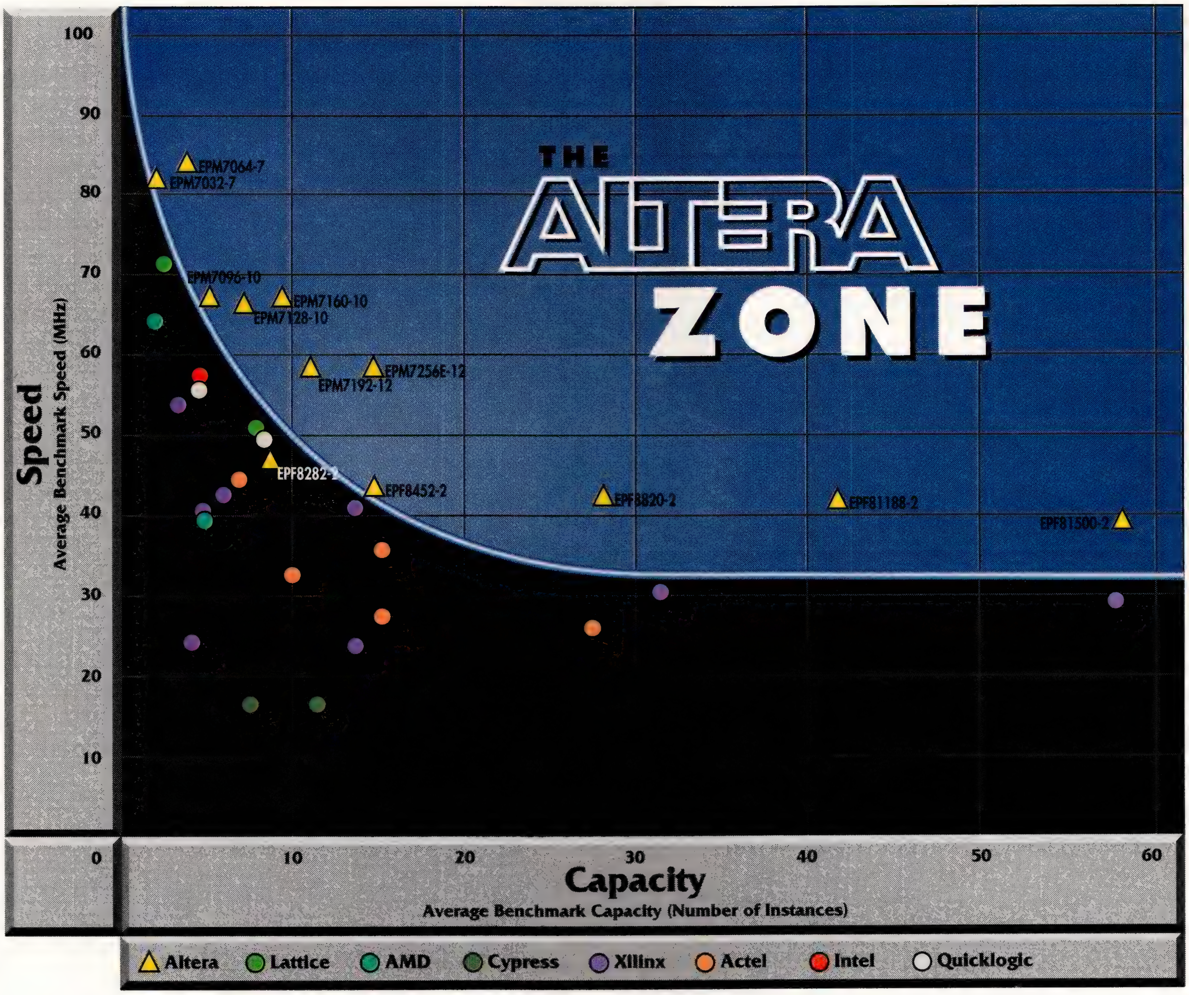
Asynchronous Transfer Mode: Bandwidth For The Future
Author/Publisher: Telco Systems
Distributor: Advanced Data
Phone: (216) 826-2839 or (800) 598-6008
Cost: $9.95 + state tax, + $5.00 shipping
An excellent introductory book to ATM. Written for engineering folks but at a less rigorous level of technical detail. Provides a good overview before diving into the depths of ATM.

ATM Over SONET: Seamless LAN/WAN Integration
Author/Publisher: IgT Inc.
18310 Montgomery Village Ave., Suite 300
Gaithersburg, MD 20879
Phone: (301) 990-9890
Cost: Free in single copies
A very good introduction to the Sonet protocol. While not an in-depth technical document, this book gives you a clear picture of the issues involved with using Sonet and other high-speed interfaces. It's easy reading and offers a good perspective of how ATM-over-Sonet attempts to bridge the gap between telecommunications and data communications.

ATM Silicon For The Information Highway—Research Report
Author/Publisher: Adger Smythe Corp., 3483 Ocean Ave., Carmel, CA 93923
Phone: (408) 622-0906
Cost: $1495 for the report, plus 1 update
Expensive but worth it. This report covers the ATM industry in depth, providing straight talk on late-breaking technology, business climate changes, standards evolution, and over-the-horizon trends. If your business surfs the cutting edge, this is a valuable information tool.

ATM User Newsletter
Jeffries Research, 2859 Stardust Dr., Santa Maria, CA 93455
Phone: (805) 934-1056
E-mail: atmuser@mcimail.com
Cost: $395/year for 12 issues
This small monthly newsletter is targeted primarily at MIS and CIO management types. However, many engineers, technology managers, and marketeers also subscribe because it provides an in-depth view of the industry from the user's perspective. Lots of insights and late-breaking news.

Once again PREP proves who owns the zone.



All programmable logic suppliers would like you to think that their devices are the fastest. Or the largest. But PREP (Programmable Electronics Performance Corporation) benchmark data has proven, for the second year in a row, that Altera is the leader in both speed and capacity.

A consortium of 13 programmable logic manufacturers, PREP was formed to create a single suite of benchmarks, allowing accurate speed and density comparisons among devices from different vendors. Once again, the benchmark results show Altera is on top in both categories. Proving that the place where you'll find the fastest programmable logic across all densities is the Altera Zone.

By choosing Altera for your programmable logic needs, you get more than speed and density. You also get technology leadership, easy-to-use design software and comprehensive technical support. This is real value. This is the Altera Advantage.

To find out more about Altera's products, and to get the most current PREP results, call us at 800-9-ALTERA (800-925-8372), or write: Altera, 2610 Orchard Parkway, San Jose, CA 95134-2020.

The ALTERA Advantage

A PREP™ COMPANY

Presentations use or include the most recent PREP PLD Benchmark data which was measured according to Benchmark Suite #1, Version 1.2 and Version 1.3. Any analysis is not endorsed by PREP.

© Copyright 1994 Altera Corporation. Altera is a registered trademark, and specific Altera device designations are trademarks of Altera Corporation. PREP is a trademark of the Programmable Electronics Performance Corporation. All other brands or products are trademarks of their respective holders. Average Benchmark Capacity is the average number of benchmark instances, and Average Benchmark Speed is the average of internal and external speeds, across all nine PREP benchmarks.

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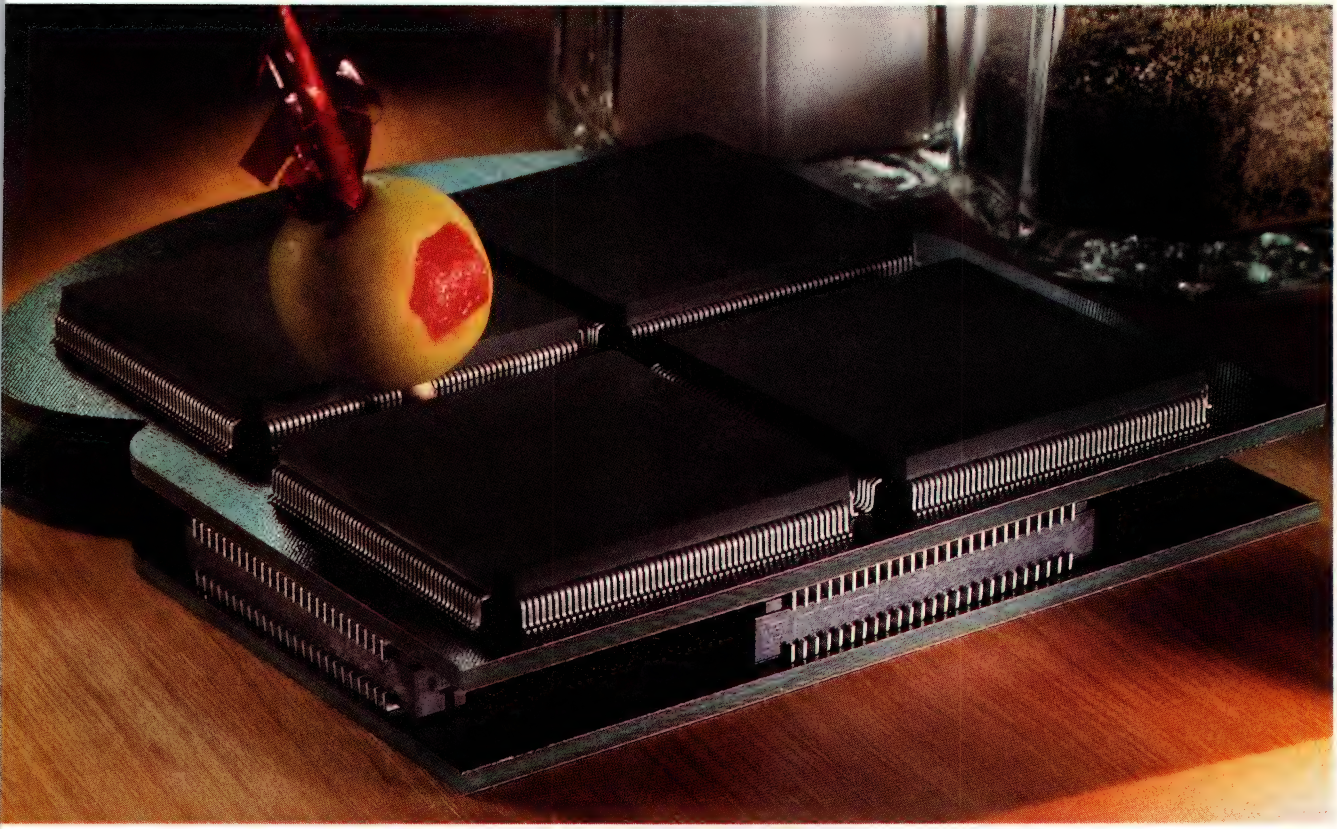
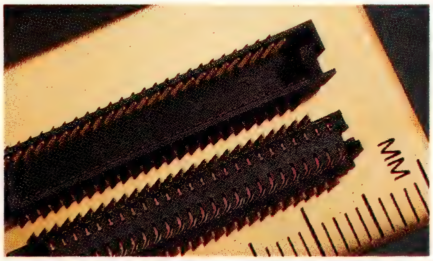
AVAILABLE ATM ICs

Vendor	Decivce	ATM Functions	Comments
Advanced Micro Devices Sunnyvale, CA (408) 732-2400	TAXI Transceiver	TAXI transceiver supports PHY/PMD layer. Bipolar chip set encodes/decodes and performs clock recovery. Capable of 200+ Mbits/s.	Switching technology in development in cooperation with Carnegie-Mellon Univ.
Analog Devices Norwood, MA (617) 329-4700	AD800, AD8002, and AD8005 PLL chips	PLL chips support PHY/PMD layer. Supports DS-3 (44.7 Mbits/s), STS-1 (51.8/155.5 Mbits/s), and STM-1 (155.5 Mbits/s) data transmission. PLLs perform clock recovery and data timing functions.	
Applied Microcircuits San Diego, CA (619) 450-9333	S3011/3012 Sonet transmitter/receiver	Supports OC-3 (155.5 Mbits/s) at PHY/PMD layer.	S3011/3012 Sonet transmitter/receiver chip set is compatible with Fujitsu, NTC, PMC-Sierra, SUNI and Integrated Telecom Sonet LAN ATM processors.
	S3005/3006 Sonet transmitter/receiver	Supports OC-3 (155.5 Mbits/s) and OC-12 (622 Mbits/s) at PHY/PMD layer.	
	AMCC3014 PLL chip	Supports PHY/PMD layer with clock synthesis and recovery to 622 Mbits/s. Receives either OC-3/STM1 or OC-12/STM4.	
	S2020/2021 switch chip	32-by-32 crosspoint switch chips for switch fabrics.	
AT&T Microelectronics Allentown, PA (800) 372-2447	T7651 transceiver	16-CAP transceiver supports PHY/PMD layer on UTP Category-3 copper at 51Mbits/s.	Other chips support PHY/PMD layer for DS-1/T-1, FDDI (100 Mbits/s), Fibre Channel (155 Mbits/s), and 622-Mbit/s Sonet.
	T7295/6 transmitter/receiver chips	Transmitter/receiver chips support PHY/PMD layer for T-3/DS-3.	AT&T builds customer proprietary ASICs for vendors and OEMs used in ATM processing applications.
	1408A/B and 1237/1261 transmitter/receiver chips	Optical transmitter/receiver chips support STS-3C Sonet at PHY/PMD layer.	
	Phoenix 2-by-2 switch matrix	Switch matrix chip is self-routing. Scalable design permits use in small and large ATM switch fabrics with data rates to 300 Mbits/s.	
	DA622MA/AM multiplexer/demultiplexer	12:1/1:12 multiplexer/demultiplexer handles data at 622 Mbits/s.	
Bipolar Integrated Technology (BIT) Beaverton, OR (503) 629-5490	Workstation interface chip	SAR functions supported by ATM workstation interface. Both SAR and scalable ATM switch technology are available for OEM license.	No chips directly available from BIT. Company licenses design technology to other manufacturers. SAR Design is Utopia-compatible.
Brooktree San Diego, CA (619) 452-7580	BT8220 transmitter/receiver	PHY/TC layer supported by transmitter/receiver chip.	Evaluation board available for BT8215. Chips support 34, 51 and 155 Mbits/s.
	BT8210 transmitter/receiver	PHY/PMD layer supported by transmitter/receiver chip. Handles SMDS.	
	BT8330 framer/formatter	HDLC framer/formatter supports PHY/TC layer. Handles DS-3 and E-3 formats.	
	CY7B923 PLL	PPL chip supports PHY/PMD layer.	
	BT18215 cell buffer	Bi-directional cell buffer facilitates transmission-rate matching for terminals, hubs and switches.	
Cypress Semiconductor San Diego, CA (619) 943-2600	CY7B933 SAR	SAR chip supports ATM layer.	Supports 160-300 Mbits/s.
	CY7B951 SST Sonet transceiver	Transceiver supports PHY/PMD layer for OC-1 (51 Mbits/s) and OC-3 (155 Mbits/s).	Full line of ATM chips in development. SST transceiver directly compatible with PMC-Sierra and IgT ATM controllers. On-chip 8X clock multiplier lowers parts count.
Fujitsu Microelectronics San Jose, CA (408) 922-9000	MB86683 network termination controller (NTC)	Supports PHY/TC layer. Frames UNI cells in DS3, E3, or Sonet format. Requires transmitter/receiver chip for wire or fiber interface at PMD layer.	Supports 45, 100, and 155 Mbits/s. Chip set supports UNI and NNI address formats.
	MB86683 NTC	Supports both ATM and PHY layers. Compatible with SDH, T3, and 155 Mbits/s.	
	MB86686 adaptation layer controller (ALC)	AAL layer supported by ALC. Includes 32/64-bit DMA controller. Supports AAL types 3, 4, and 5.	
	MB86680 4-by-4 self-routing switch element (SRE)	4-by-4 SRE can be used to build small and large switch fabrics.	
	MB86689 address translation controller (ATC)	ATC can pass routing information directly from NTC to the SRE via a proprietary interface.	

How to sandwich more on a motherboard.





With real estate at a premium, designers are hungry for new ingredients in the recipe for high-density packaging.

Enter the tasty AMPMODU Metristak interconnect family, from AMP. Designed for parallel board-to-board stacking on 1.0mm centerlines, Metristak connectors offer very high density — with very distinctive features.

An innovative tongue-and-groove contact design overcomes the limitations of pin-and-socket connectors, with co-planarity that exceeds industry standards. The exceptionally short electrical path (50ps) supports demanding data rates. Simple in design and inexpensive to produce, Metristak connectors are also inherently rugged; add our special housing features, and they integrate easily with your vacuum nozzle or robotic pick-and-place machinery.

And small as they are, they're long on user-friendliness. Post guides and polarizing features allow easy blindmating — critical in tight spaces (or, for upgradable designs, in the hands of end users). Metristak connectors come on standard EIA481 carrier tape, ready for uncomplicated manufacturing. We'll help there, too, with the technical support you need.

And if you need help in more ways, we offer services that range from design verification to board layout, fabrication to complete systems — taking full advantage of design breakthroughs like the Metristak interconnect family.

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Scandinavia: Sweden 46-8-580-833-00 (fax 46-8-580-194-70)
Central Europe: Holland 31-73-20-0911 (fax 31-73-21-2365); Germany 49-6103-7090 (fax 49-6103-709223); Great Britain 44-81-954-2356 (fax 44-81-954-6234)
Southern Europe: France 33-1-34-20-8888 (fax 33-1-34-20-8600); Italy 39-11-401-21111 (fax 39-11-403-1116); Spain 34-3-200-8466 (fax 34-3-201-7879)

AMP

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while still maintaining a fixed time relationship between data cells. While not critical with conventional data transmissions, this "isochronous" characteristic becomes very important for time-sensitive transmissions such as real-time voice and video.

To better understand how ATM silicon ICs differ, it's important to know how the ATM protocol works. First, let's take a closer look at the functions performed by ATM.

Like most data-communications standards, the ATM protocol follows the 7-layer Open Systems Interconnection (OSI) reference model of the International Standards Organization (ISO). The protocol covers the reference model's layer 1 (the physical-medium layer) and layer 2 (the link layer). Within the two layers, the ATM protocol further separates the functions it performs into sublayers *(Fig. 1)*. The model, developed jointly by the ATM Forum and the TSS section of the International Telecommunications Union (ITU), identifies an ATM adaptation layer (AAL), an ATM layer (ATM), and a physical layer (PHY).

The AAL is the bridge between data in its native form and the ATM network. Within the AAL, data from a source (a workstation, a PC, or another LAN) is broken down for transmission into 48-byte "payloads." When receiving ATM packets, the AAL is responsible for reassembling the data to its original form. This process is often referred to as segmentation and reassembly, or SAR.

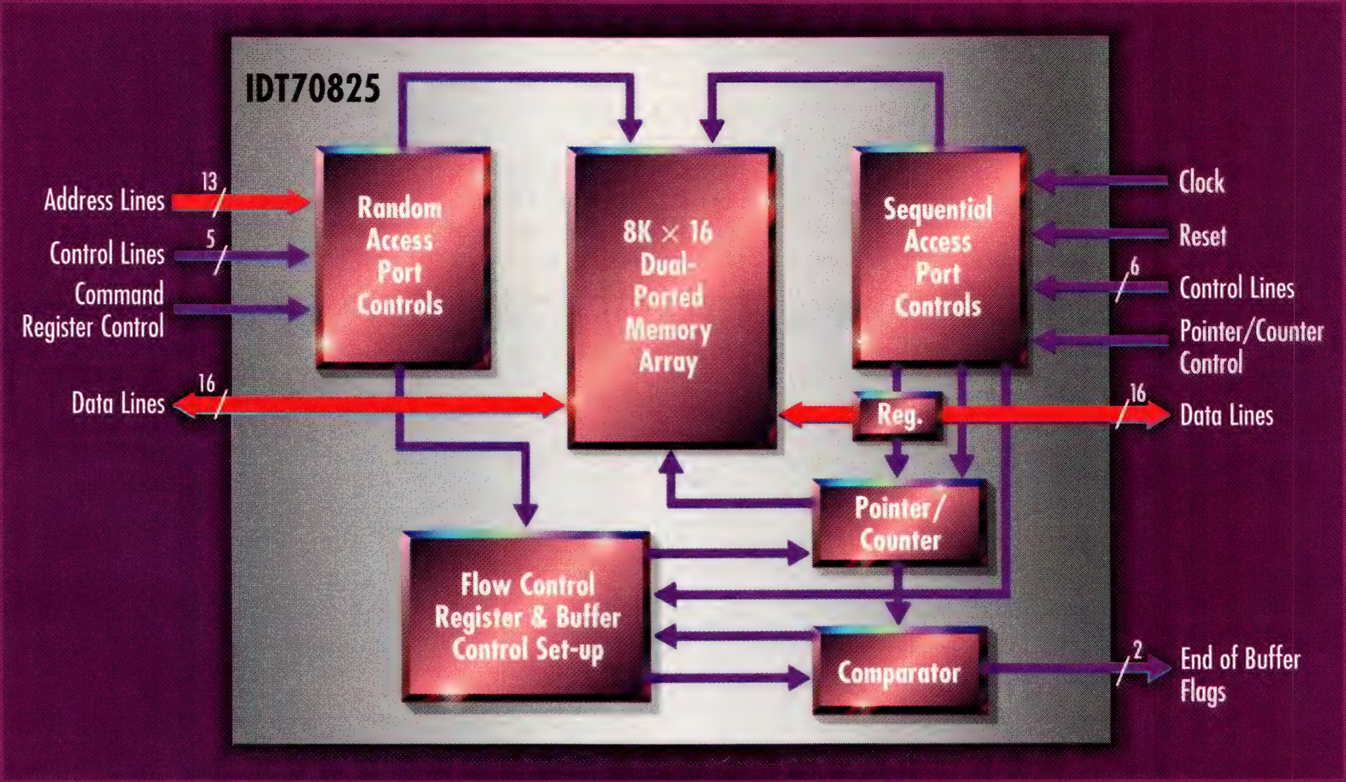
The AAL passes the payload segments through the ATM layer (ATM), which adds a 5-byte header that contains the requisite routing and control information required to get the packet to its destination. The

AVAILABLE ATM ICs

Vendor	Decivce	ATM Functions	Comments
Integrated Telecom Technology (IgT) Gaithersburg, MD (301) 890-9890	WAC-034-A and WAC-013-A framer/formatters	Framer/formatters support the PHY/TC layer. WAC-034 frames cells in DS-3, E-3, and E-4 format. WAC-013 frames cells in Sonet format at all rates to 155 Mbits/s.	PHY/TC devices are fully compliant with Utopia interface standard. ATM layer SAR function chip anticipated later this year.
	WAC-011-A HDLC controller	HDLC controller performs protocol conversion between ATM cells and HDLC packets. Can be used to build devices which bridge ATM and HDLC networks.	Switching function chips anticipated later this year. Low-cost, PC-based ATM test system provides test data stream and analysis for product development and network troubleshooting.
IBM Research Triangle Park, NC (919) 543-5221	Transceiver and SAR chips under development	Transceiver will support PHY layer. SAR chip will support ATM layer.	Board-level solutions also available.
	Prisma 64-by-64 switching chip available soon	64-by-64 switch-chip architecture is scalable and uses a low-latency self-routing scheme. Bi-directional data rates up to 8 Gbits/s.	
LSI Logic Milpitas,CA (408) 433-8000	No standard chips available. Custom ASICs can incorporate ATM functions from standard-cell library.	ATMizer ASIC logic core supports entire ATM layer. ATMizer ASIC logic core supports PHY-TCS sublayer. Cascade ASIC logic core can provide on-chip ATM-to-Ethernet translation. SierraLink ASIC core supports high-speed optical or copper signals. Fibre Channel Standard (FCS) ASIC core can be used to translate between ATM and Fibre-channel protocols. Other ASIC cores or external transmitter/receiver circuits can be used for the PHY-PMD sublayer.	Custom ASICs with ATM processing and specialized interfaces can reduce parts count, volume, power, and costs for medium-to-high-volume production applications. Reprogrammable processor in ATM interface permits firmware updates as product requirements or ATM standards evolve.
Micro Linear San Jose, CA (408) 433-5200	ML-6672 transceiver	Supports PHY/PMD layer on UTP Category-5 copper at 155 Mbits/s.	Optical transceiver can handle up to 155 Mbits/s at distances to 100 m.
	ML-6633/6622 optical transmitter and receiver	Transmitter and receiver chips provide optical fiber PHY/PMD interface.	Support of Category-5 UTP copper opens up low-cost ATM connections to the desktop.
National Semiconductor Santa Clara, CA (408) 721-5000	DP83223 Twister	Twister chip supports PHY/PMD layer using Category-5 UTP copper at 155 Mbits/s.	Twister offers UTP Category-5 copper interface that lowers the cost of a desktop ATM connection.
	DP83372 FRED ATM transmitter	FRED chips support SAR/ATM layer. Utopia-compatible with PHY layer using minimal glue chips. Supports AAL 2, 3, 4, and 5.	Board-level solutions also available.
	DP83382 FRED ATM receiver		
NEC Mountain View, CA (800) 366-9782	μPD98401	Supports AAL and ATM layers for AAL 1, 3, 4, and 5.	Two-chip ATM interface for workstations, servers, etc. Chip set supports Sonet STS-3 protocol.
	μPD98402	Chip implements PHY/TC layer. Supports STS-3C (155 Mbits/s) Sonet. Both chips are Utopia-interface compliant.	Adaptation-layer generic 32-bit DMA interface simplifies CPU interfacing.

Sa·ram (Sə-răm′)

Definition: *noun.* 1. A new innovative Sequential Access/Random Access Memory chip from IDT. 2. The combination of a FIFO and Dual-Port memory on one chip. 3. A real estate saving chip that makes your life easier. 4. The fastest and largest Multi-Port SRAM in the semiconductor industry.



IDT defines your next specialty memory!

A Combination FIFO and Dual-Port

IDT's innovative new SARAM™ combines the advantages of a synchronous FIFO and dual-port SRAM in one chip. It offers the functionality of a bidirectional synchronous FIFO on one port and the asynchronous random access capability of an SRAM on the other while maintaining a true dual-port's ability to simultaneously access data in a given memory cell from either port.

Configurable Buffer

The 8K × 16 SARAM is comparable to the largest dual-port available, so large packets of data can be transported in applications such as telecommunication switches, bridges, and routers. SARAM's large configurable buffer allows designers to customize the buffer size on-the-fly for each application.

25ns Access Time

IDT's SARAM allows memory accesses as fast as 25ns on either port. At top speed with both ports active, SARAM consumes as little as 1.5W of power; when idling, SARAM consumes as little as 25mW. Best of all, SARAM is packaged in a low-profile 80-pin TQFP package, so you save significant board space both in part count and package size.

Free Pocket Dictionary

Call or FAX us today and receive a free pocket-size Webster's dictionary and bookmark, SARAM data sheet, application note and a sample request card so you can begin designing with IDT's innovative SARAM dual-port memory now!

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header also contains space for an 8-bit header error-control code (HEC), which is used to verify the integrity of the header data.

Another function of the ATM layer is to multiplex the packets onto their virtual channels and assure sequential delivery of packets. This layer also monitors such performance criteria as cell errors, cell loss ratio, and cell transfer delay. These parameters then are passed to whatever device controls the transmission procedurefor analysis and corrective action.

Once the ATM packets are created, they're passed to the transmission-convergence (TC) sublayer within the PHY layer. First, a HEC is generated and inserted into the cell. Next, the outgoing cells are mapped, or arranged into groups that are compatible with the physical transmission format. Finally, in the physical-medium-dependent (PMD) sublayer, cells are buffered to match the allocated rate of the data stream and converted into either an optical or electrical signal for transmission. When data is received, the PHY layer synchronizes the bit-stream and recreates the packets in a process known as cell delineation.

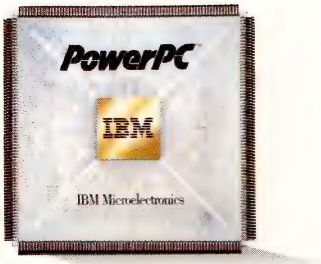
Makers of ATM processing chips have taken several approaches to dividing up the job responsibilities of each ATM layer between their chips. Therefore, the structure of an ATM chip set says much about what kind of performance it can deliver. Because manufacturers employ a number of different algorithms, selecting the proper SAR chip can greatly affect system throughput and overall performance. In addition to raw performance and physical-layer compatibility, the advantages offered by a particular chip set's divi-

AVAILABLE ATM ICs

Vendor	Decivce	ATM Functions	Comments
PMC-Sierra Burnaby, BC, Canada (604) 668-7300	PM 7345	Supports PDH at PHY/TC layer for DS/E-3.	Additional chips that support all ATM layers are in development.
	PM 7321	Supports SMDS at PHY/TC layer for DS/E-3. Adapter chips allow DS/E-1 operation.	
	PM 5345/6	Chips support PHY/TC layer for DS-1/3 over Sonet.	
	PM 5318	Serial parallel converter handles 622 Mbits/s.	
	PM 5321	Terminating transceiver interleaves four 155-Mbit/s data streams into a 622- Mbit/s Sonet signal.	
Texas Instruments Dallas, TX (214) 995-2011	TDC 1560	Supports ATM- and AAL-layer interfaces for SBus-based computers.	Chip set jointly developed by TI and Sun Microsystems.
	TDC 1500	Transmitter/receiver provides PHY/TC interface for STS-3C (155-Mbits) Sonet.	Both chips are compatible with Utopia-interface standards.
			SBus board-level solution available through Sun.
TranSwitch Co. Shelton, CT (203) 929-8810	TXC-05501/5601	SAR chips support ATM layer.	Other modular ATM system blocks include the Overhead terminator, De-jitter buffer, and Sonet mapper.
	TXC-05150	Cell-delineation-block (CDB) processor supports the PHY/TC layer for DS-1/3, E-1/2/3, STS-1/3C, and STM-1.	Modular segmentation of ATM functions within chips permits flexible approach for specialized applications such as add/drop multiplexers and data concentrators.
	Cubit switch-fabric cell	CelBus-based self-routing switch-matrix chip provides a scalable building block for routers, multiplexers, bridges, and small-to-medium-size switching fabrics.	Two-chip and single-chip node interfaces are under development.
TriQuint Semiconductor Beaverton, OR (503) 644-3535	TQ8016	16-by-16 crosspoint switch. Supports data rates to 1.3 Gbits/s.	TriQuint also produces ASICs that employ standard cells that support ATM/PHY layer for Sonet at data rates of OC-3 (155 Mbits/s) through OC-48 (2.4 Gbits/s).
	TQ8032	32-by-32 crosspoint switch. Supports data rates to 800 Mbits/s.	GaAs technology provides high-speed ASICs and standard products. Product line due to expand to meet anticipated market for high-speed ATM devices.
VLSI Logic San Jose, CA (408) 434-3000	Custom ASIC supplier. No standard chips currently in production.	No standard ATM chips available. But VLSI does offer several functional standard blocks (FSBs) for their ASICs that perform ATM functions. Current offerings include T1/E1 support at the PHY/PMD layer, a 155-Mbit/s I/O cell, and clock synthesis.	ASICs can provide a cost-effective approach for incorporating ATM technology into medium-to-high-volume products.
		FSBs under development include T1/E1 transmit/receive cell framers, and Sonet transport overhead processor cells.	Currently working with Efficient Networks Co. and several other customers on ATM chips.

HDLC = high-level data-link control; NNI = network-to-node interface; PHY = physical layer; PMD = physical-medium-dependent sublayer; SAR = segmentation and reassembly sublayer; SMDS = switched megabit data service; UNI = user-to-interface network; Utopia = universal test and operations interface for ATM.

Congratulations, Apple, on a day we've both looked forward to seeing.



IBM Microelectronics
Total Technology Solutions

On March 14th Apple launched Power Macintosh™ systems, a family of personal computers using our revolutionary, RISC-based PowerPC™ microprocessors. As a member of the PowerPC alliance with Apple and Motorola, we're proud to see such tangible proof that our vision has become a reality. Yet while IBM is delighted to celebrate today, we're still determined to anticipate tomorrow. With products, applications and support designed to make PowerPC microprocessors, and the systems they run, the future of computing. It's a challenge IBM Microelectronics™ Division and Apple welcome. In fact, we look forward to it.

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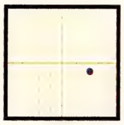
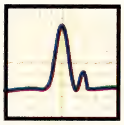
Get a sample of reality.

Looking for analog confidence in a digital oscilloscope? Tektronix' TDS 350 sets the standard with Digital Real Time. ■ Its incredible *one gigasample/second* sampling delivers real-life capture like never before—both for single shot or repetitive events. Select peak detect for slow events, or push the scope to its full 200 MHz bandwidth—with no aliasing. ■ And, like the entire TDS 300 family, the TDS 350 sets a new standard in price/performance: under $4000.



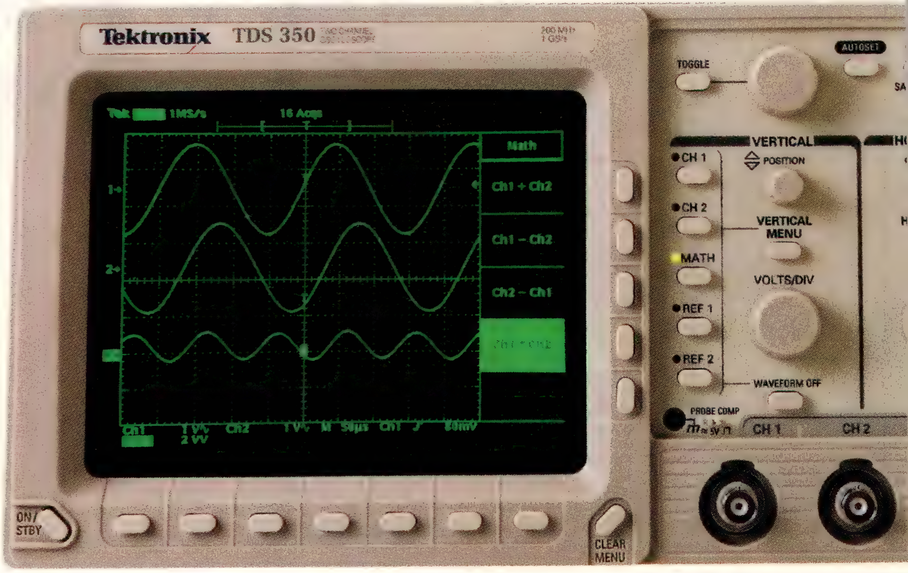
One Point Captured. Single event capture using Equivalent Time Sampling. 20 MS/s 100 MHz DSO.



Real Life Capture. Single event capture using Digital Real Time. 500 MS/s 100 MHz DSO.

Analog look and feel. The TDS 300 family is simple and intuitive; just like your trusty analog scope. Even the digital interface is simplified with on-screen icons. You may never have to crack open the instruction manual!

High-end digital features. Each model features over 20 automatic measurements. Continuous update for hands-free operation. Four acquisition modes and video trigger—perfect for tailoring the display. And a communication option for hardcopy to most printers, or to send/receive waveforms and setups.



There's a TDS 300 Series scope for every application. And every budget.

FEATURES	TDS 310	TDS 320	TDS 350
Bandwidth	50 MHz	100 MHz	200 MHz
Max Sample Rate	200 MS/s/chan	500 MS/s/chan	1 GS/s/chan
Sweep Speeds	10 ns/div - 5 s/div	5 ns/div - 5 s/div	2.5 ns/div - 5 s/div
Channels	2	2	2
Vertical Sensitivity	2 mV - 10 V	2 mV - 10 V	2 mV - 10 V
Vertical Resolution	8 bits	8 bits	8 bits
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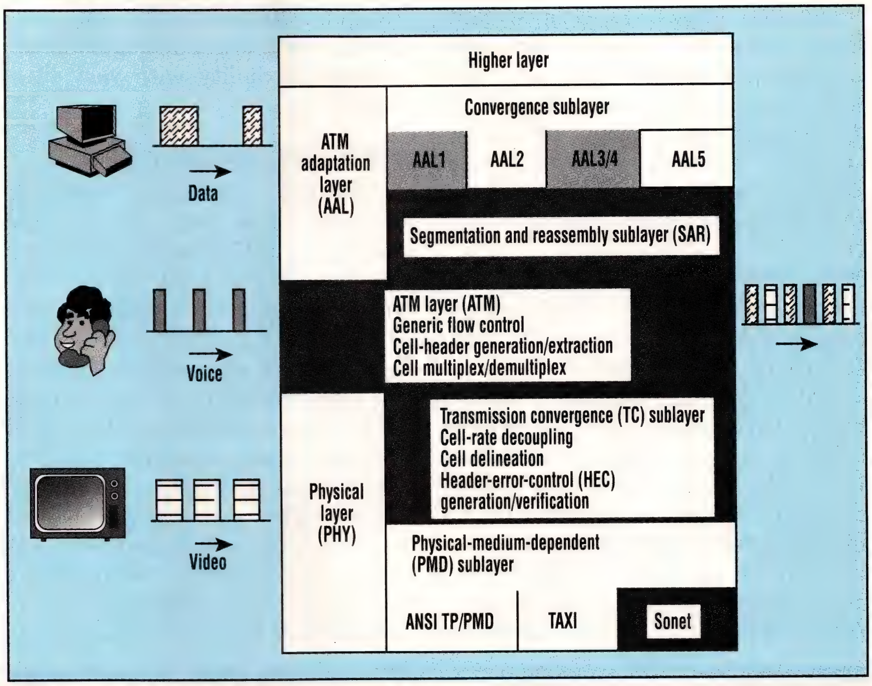
sion of tasks will be a major factor in selecting a product for a specific application.

At the AAL, some manufacturers have developed an interface that maps the ATM-cell data directly into the architecture of the target system. As an example, the chip set developed jointly by Sun and TI provides a direct path to the SBus used by Sun workstations.

Another good example of a specialized AAL interface is the Cobra AAL processor developed by TranSwitch. It permits up to four T1 (1.544-Mbit/s) or E1 (2.048-Mbit/s) telecommunications lines to be interfaced directly to an ATM channel. More often, however, a generic interface is provided so that it's usable in a wider range of applications. Concerning the chip set offered by NEC *(see the table, again)*, the manufacturer supplies a 32-bit DMA system that allows for a simple interface to most processors using a few additional glue-logic chips.

Several issues must be considered when selecting components for the ATM-layer functions. Although at first glance it may seem that the ATM layer is simply responsible for "packaging" the data, much more happens here. For instance, an output queue buffers the data flow and keeps it within the assigned bandwidth of the virtual channel. On the input end, cells are pushed onto a FIFO buffer until they can be passed to the AAL. While some chips employ an on-chip buffer, such as those from Fujitsu and Integrated Telecom Technology (IgT), other manufacturers employ an external RAM chip for this function. It's a less integrated solution, but the external buffer may be desirable if the anticipated traffic has frequent burst rates far above the preferred channel bandwidths.

At the PHY/TC layer, ATM information can be transmitted via either optical fibers or copper wire. For short hauls in multiple-node applications, copper is usually the best choice due to the lower overall cost and ease of installation. Using existing technology, data rates of up to 155 Mbits/s can be transmitted over unshielded, twisted-pair (UTP) wires for distances of up to 300 meters.


Higher layer
Convergence sublayer
ATM adaptation layer (AAL)
AAL1
AAL2
AAL3/4
AAL5
Data
Segmentation and reassembly sublayer (SAR)
ATM layer (ATM)
Generic flow control
Cell-header generation/extraction
Cell multiplex/demultiplex
Voice
Transmission convergence (TC) sublayer
Cell-rate decoupling
Cell delineation
Header-error-control (HEC)
generation/verification
Physical layer (PHY)
Video
Physical-medium-dependent (PMD) sublayer
ANSI TP/PMD
TAXI
Sonet

1. THE ATM PROTOCOL STACK is a switched, multiplexed protocol that permits transmission of mixed signals. Modular layers provide a seamless interface to a variety of transmission media. (Source: NEC Electronics).

The PHY/TC layer definition offers several ways to prepare the digital content of cells for conversion into robust analog data streams and to recover data at the other end. Sonet and T1/E1 pleziochronous-digital-hierarchy (PDH) mapping techniques use the HEC byte in the header as a synchronization mark to reassemble data cells. The Sonet mapping process assembles ATM cells into fixed-size frames along with additional embedded control and error-detection bytes.

Although Sonet is a very complicated protocol, several vendors, including IgT, PMC-Sierra, TranSwitch, and TriQuint Semiconductor offer single-chip framers. In return for the added complexity, Sonet offers high noise immunity, a wide variety of data rates ranging from fast (51 Mbits/s) to blazing fast (2 Gbits/s), and standards that permit transmission over either optical fiber or UTP copper. Using Sonet at the end node also carries with it the advantage of encapsulating data in a WAN-compatible form. And, using Sonet in local networks can eliminate the need for further protocol conversion when bridging to other types of LANs or WANs.

Also defined for ATM applications at the PHY/TC layer are 4B/5B TAXI coding and 8B/10B Fibre-Channel coding. Classified as explicit delineation techniques, these coding schemes insert previously defined characters that define the start of cells and the space between cells into the data stream. These simpler formats usually are adequate for local applications and are supported by many chip manufacturers.

Much activity is occurring at the PHY/physical-media layer, with many vendors offering transceiver chips for both fiber and copper. Such companies as Advanced Micro Devices, AT&T, Brooktree, and TriQuint Semiconductor provide chips for Sonet transmission. For 4B/5B type coding, the ATM Forum specified an adaptive modulation scheme known as 16-CAP. This signal format offers high noise resistance in noisy conditions over low-quality twisted-pair wires at up to 155 Mbits/s. AT&T and Micro Linear currently offer 16-CAP transceivers.

Because so many solutions are available at the PHY layer, it's conceivable that even a single LAN may include two or more types of transmission media. To simplify the interface between the ATM and PHY layers, the ATM Forum defined a signal convention known as Utopia. The Utopia interface provides separate transmit and receive data paths as well as control handshake lines *(Fig. 2)*. In addition, Utopia provides a standard interface with which the system processor can set control parameters and perform basic self-test functions within the PHY layer. Many companies making ATM products have adopted the Utopia interface, and it is rapidly becoming a de facto industry standard.

National Semiconductor's Vicksburg ATM-adapter card is a good example of the advantages inherent in Utopia-based products. By using standard interchangeable Utopia modules, the Vicksburg board can be configured to support both copper and fiber interfaces at several data rates and encoding formats. Incorporating the Utopia interface into a design can provide a high degree of application flexibility with very little added cost.

SWITCHING TECHNOLOGY

Establishing connections, or switching, is a fairly complicated process in the ATM world. Although complicated, the ATM routing convention is logical, consistent, and provides for the efficient set up and tear down of the virtual channels that form the heart of the technology. To begin to understand how ATM switching works, it's important to remember that ATM is based on a hierarchical structure. Within a layer of the hierarchy, each switch need only know the addresses of its immediate neighbors and the address of its contact point in the layer above. If an unfamiliar address is passed to a switch node, it passes it up to the next layer of the switching hierarchy for resolution.

As noted previously, the ATM layer is the point at which the routing information is placed into the header. In a switched network, establishing a virtual connection is much like placing a telephone call. The "name" of the virtual connection assigned to the cell is arranged ahead of time while the virtual channel is being established, and commands are passed ahead of time to the switching network for execution before transmission begins. This signaling is accomplished over special virtual channels established between switches, called "meta-signaling channels." These channels are invisible to the normal data streams and are used to carry

BOARD-LEVEL ATM SOLUTIONS HAVE ARRIVED

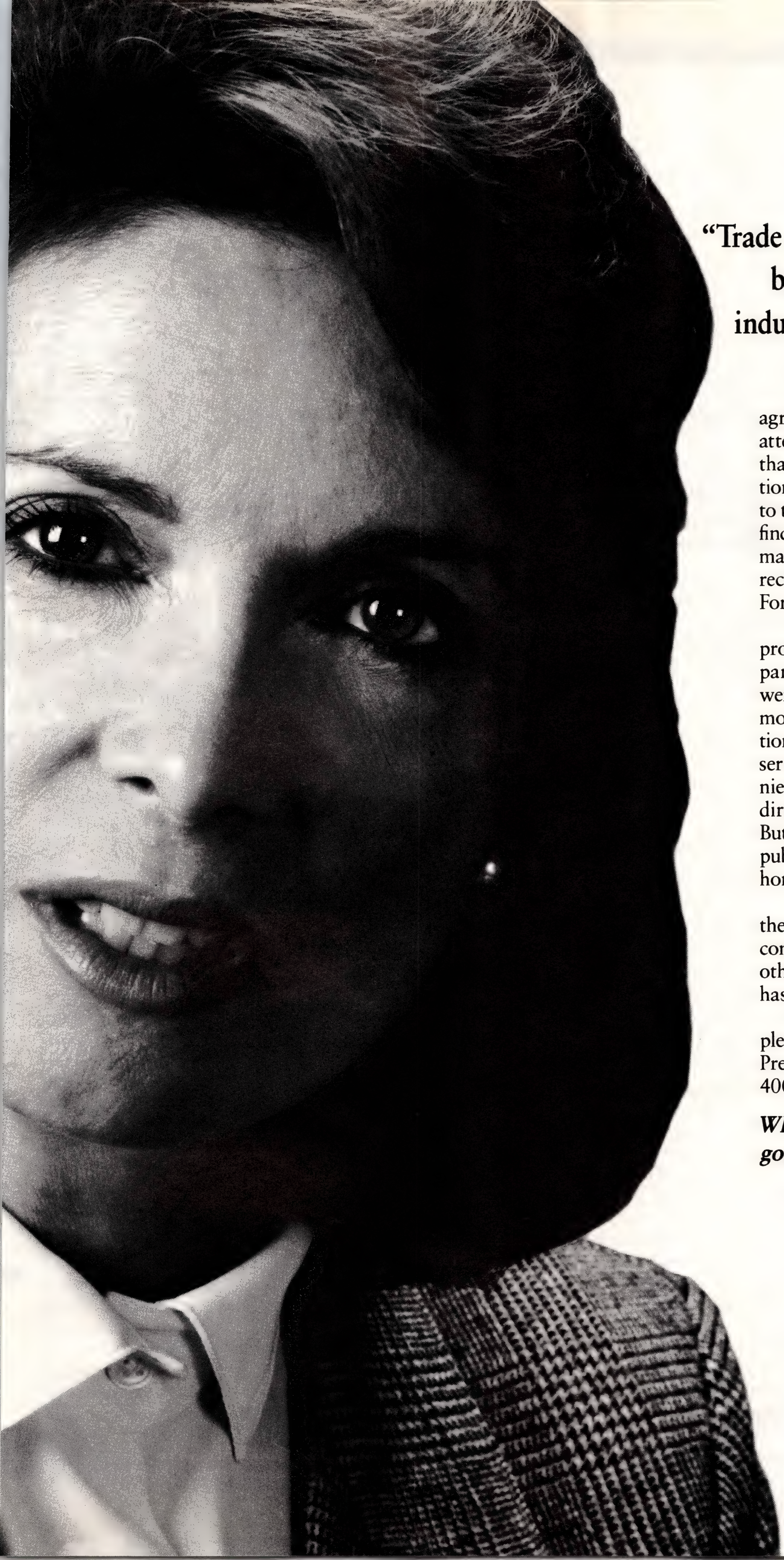
As the ATM environment becomes more common, many designers will be challenged with providing ATM capability for small-to-medium-volume products, as well as retrofitting the computers, workstations, and communications equipment in their existing infrastructure. For many applications, the choice of buying a pre-engineered ATM adapter board can save both development time and money. A raft of ATM adapter-board vendors are coming on the scene with products that support most of the common computer buses, including the SBus, the VMEbus, and even the plain-vanilla standard PC buses such as ISA and EISA. Even as this article goes to press, several manufacturers have announced their entry into the field.

When choosing a board-level solution, it's important to remember that interface software is an important (and potentially more troublesome) part of making a product ATM-capable. For this reason, most manufacturers offer driver software for their cards. Because some buses support several operating systems, it's advisable to make sure the driver supports the one that's being used. Because a general-purpose driver can't meet every application requirement, such manufacturers as Fore Systems offer software development tools to assist you in "rolling your own."

While not a complete listing, the following sampler will give you a taste of things to come:

AVAILABLE BOARD-LEVEL ATM PRODUCTS

Company	ATM board-level product
Efficient Networks Dallas, TX (214) 991-3884	Hardware and software for ATM networking. Soon to be released is the first generation of ATM adapter boards for PCI-bus, SBus and GIO (Silicon Graphics) computers. With the proprietary "Midway" SAR chip, boards will support 155-Mbit/s data rates using Sonet over optical fiber and Category-5 copper. A high level of software support will accompany each board, including functional libraries of applications programming interfaces (APIs) to facilitate interface development.
Fore Systems Warrendale, PA (412) 772-6600	ATM cards for EISA, VME, Hewlett-Packard, Silicon Graphics, and Sun machines. A PCI-bus card is under development. Cards support ATM using transparent TCP/IP adaptation software. Driver software and an application programming interface is available for most boards.
IBM Research Triangle Park, NC (919) 543-7046	Adapter boards for Microchannel, PS/2, and ISA bus machines with others to follow. Present boards operate at 25 Mbits/s, a rate not supported as a standard by the ATM Forum. All boards come with driver software. Cards that support higher data rates are under development.
Interphase Corp. Dallas, TX (214) 919-9000	The 4615 SBus card and 4625 VME card feature a modular physical-layer interface adapter. Current PHY-layer support is 100 Mbits/s over optical fiber. Other modules will be released soon to provide interfaces for optical fiber and UTP copper at 51 and 155 Mbits/s. Software drivers for Sun and Solaris operating systems are available now. Additional drivers to be released soon.
National Semiconductor Santa Clara, CA (408) 721-5000	The Vicksburg. An EISA bus card with interchangeable Utopia-compatible plug-in I/O modules to support several different PHY-layer connections. PCI board in development. Driver software for Windows NT and other systems is available.
Sun Microsystems Mountain View, CA (415) 960-1300	An SBus adapter that supports 155-Mbit/s Sonet communications over multi-mode optical fiber. A companion board that supports 155-Mbits/s over Category-5 UTP copper is scheduled for release in August of this year. Drivers for these cards are available for any Solaris operating system of level 2.3 or higher.
SynOptics Santa Clara, CA (408) 988-2400	The LattisCell ATM adapter card provides SBus-based workstations with a 155-Mbit/s ATM interface. Supporting Sonet over optical fiber or Category-5 copper, the board is directly compatible with SynOptics' LattisCell ATM switch. Cards to support other popular computer buses are under development.



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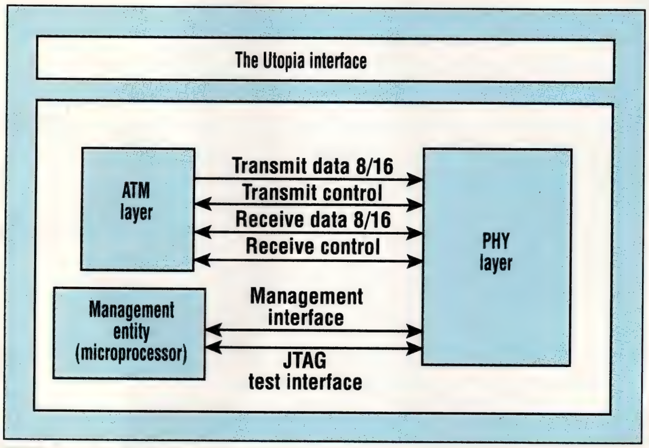

2. THE UTOPIA (universal test and operations interface for ATM) standard provides an electrical and logical interface between ATM and PHY layers.

the conversations between switches that establish and tear down the data paths between nodes as needed.

For intra-switch routing between two nodes attached to the same switch, the cell is received and passed to the ATM layer. There, it's shunted through the switch fabric to another node. Within the switch, a header routing tag is generated to tell the switching circuit where to place the cell. This tag can be transmitted to the fabric over a separate control bus or as a series of specially identified control bytes embedded within the data stream.

Some companies like Fujitsu and TranSwitch implement intra-switch routing by generating small control words that are placed between incoming ATM cells by an address-translation controller chip. Using such a method requires that the switch fabric support the proprietary signaling scheme. Though using this embedded signaling technique requires a commitment to a single vendor's line of components within the switch, it doesn't affect any aspect of inter-node or inter-switch communication. Before the ATM stream leaves the switch, the routing tag is removed from the flow, leaving only standard ATM cells. For inter-switch routing between two or more switches, the transmitting switch may or may not insert new routing information into the cell header and pass it on.

Many manufacturers currently offer chips that can be used to make a switching fabric. They fall roughly into two categories: bus-based and crosspoint-based architectures. Small-to-medium scale switches incorporate bus-based switching schemes that offer the advantage of ease of implementation. For example, TranSwitch's Cubit modular ATM-cell switching chip and its address header-controller chip provides design engineers with easy-to-use building blocks for designing low-cost, small-to-medium-sized network devices. The two chips employ TranSwitch's proprietary CellBus technology, which is a cascadable bus-based architecture. Using the technology, the switching chip can support an aggregate data rate of up to 1 Gbit/s. As switch size grows, however, crosspoint architectures can offer much higher bandwidths and matrix sizes.

In either case, the data is passed into its proper place in the output matrix after the routing information in the cell header is read and translated. Switch-fabric architecture varies greatly in bandwidth and sophistication. Simpler schemes are designed around handling a single type of data efficiently, such as desktop video, but aren't optimized to handle high-density, mixed signals. Some of the simpler switch chips aren't designed to read the AAL code in the cell headers to resolve priority between different types of data. In dense, bursty environments, this may mean that some high-priority cells may be dropped by the switch instead of shedding lower-priority cells first.

The buffering of data-switching queues may be done at either the input or output. Due to the high data rates involved, buffer RAM space is measured in megabytes and is usually a group of chips, externally co-located with the switch. Although it uses more memory and is slightly more complicated, output buffering usually is better because it ensures that data won't be lost as long as sufficient buffer RAM is in place.

Speaking of buffers, remember that as traffic gets denser (which makes it subject to high-rate bursts), larger amounts of fast buffer memory are required. Currently, most first-generation ATM switching devices are designed to use expensive static RAM. As switching networks grow larger, the cost of RAM may prove to be the limiting factor for bandwidth and channel capacity unless a way to use less-expensive dynamic RAM is developed.

Using the current ATM standards for signaling, switched virtual channels may be established between any two points within a private ATM network. Still, a problem arises when attempting connections through public networks, such as across telephone lines or between two private networks. At the time this article was written, the more complicated standards for signaling through public networks was nearly complete but not implemented. For this reason, communication over public networks is still handled through permanent virtual channels that are set up manually by a network manager and dedicated for a given period of time, regardless of whether or not there's traffic.

Using a permanent virtual channel is analogous to leasing a T1 or T3 line from the telephone company, where you usually buy more capacity than you need for longer than you need. Once the standard for public switched virtual circuits is established by the ATM Forum (probably in early 1995), ATM is expected to approach its full potential. Until then, it can still be used as a highly efficient transport medium within private LAN and WAN environments.

THE ELUSIVE SINGLE CHIP

For engineers designing portable or high-volume products, reducing parts count is a high priority. Toward this end, several manufacturers have concentrated their efforts on cutting the number of chips required to give ATM capability to a personal computer, file server, or workstation. Although the technology is still in its infancy, competition for a share of this potentially huge market is intense. Several companies are expected to release their "single-chip solution" to ATM interfaces by the end of this year. While no one-chip solution exists today, companies like Fujitsu, NEC, and Texas Instruments offer two-chip solutions that span the AAL, ATM, and PHY layers.

Be aware that the much sought-after, one-chip ATM processor isn't a panacea for all applications. While one- or two-chip solutions are great for high-volume products such as workstations, their design usually only supports a specialized AAL interface that may be unsuitable for a different product. In addition, these "complete solutions" usually span the entire set of ATM layers, something that might not be necessary. As an example, ATM switches and routers don't need to reassemble packetized data into its original format; they simply act as conduits for packets at the ATM layer.

Remember, too, that ATM data is carried by so many different PHY-layer interfaces that it certainly isn't cost-effective or possible for chip makers to support all of them as integrated solutions. For the time being, expect to see at least some of the PHY-layer interfaces supported by external chips, especially for complex transmission schemes like those used by Sonet.

CUSTOM ATM ASICS

In cases where chip count is critical, due either to cost or space constraints, it will soon be possible to fabricate a custom chip that incorporates some or all of the ATM processing functions, along with custom logic that's tailored to a specific application. Several firms, including LSI Logic, TriQuint Semiconductor, and VLSI Technology, have developed standard cells for various ATM functions. These manufacturers are rapidly adding ATM functions to their menus, anticipating the need for custom ATM interfaces in low-cost, high-volume equipment (terminals and multimedia processors, for example).

When designing a network-based product, an ATM interface option should be considered if it's expected to routinely transfer large amounts of high-speed data. The types of networks it will be required to operate on must be carefully examined before selecting a PHY-layer interface. In this case, using the Utopia standard would be a good choice because it provides for easy upgrades at the PHY layer. Finally, several different vendor approaches to ATM should be looked at to ensure that the right amount functionality is purchased. Careful matching of chip-set capability to system requirements is a key aspect in developing a cost-effective solution.☐

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DESIGNERS CREATING MIXED 3-V AND 5-V SYSTEMS NEED TO BE FAMILIAR WITH A FEW BASIC ISSUES TO AVOID FUTURE TROUBLE.

TIPS FOR STRADDLING THE 3-V TO 5-V FENCE

Quite a few articles have been written about transitioning from 5- to 3-V systems. Basically, the stories state that 3-V systems can reduce power consumption by 50% or more, and that the lower supply potential lets IC manufacturers use tighter device geometries to create faster, denser chips. Some suggest that because this transition will be gradual, mixed 3- and 5-V systems could become common. After all, the voltage levels representing logic-low and logic-high on a 3-V CMOS part are compatible with those of a 5-V TTL part.

However, it seems as though whenever reference is made to mixing 3-V and 5-V systems, warnings about "special design considerations" crop up that may be a little unclear to those having to deal with such considerations. As a designer of TTL-compatible 3-V ICs, I'd like to discuss some of these issues in the hope of saving someone a few headaches.

Mixing 3-V and 5-V systems isn't difficult. However, designers of such systems do need to be familiar with a few basic issues or they may get themselves into trouble. I've been approached by a number of designers at conferences with questions, but most aren't patient enough for a complete answer. They will interrupt with something like "Look, all I want to know is can I drive this 3-V CMOS input with a FAST output or not?" They hate it when I answer "Yes, you can, but..." Unfortunately, to design a mixed 3- and 5-V system that behaves as expected, designers must understand the "why" and not just the "what." This

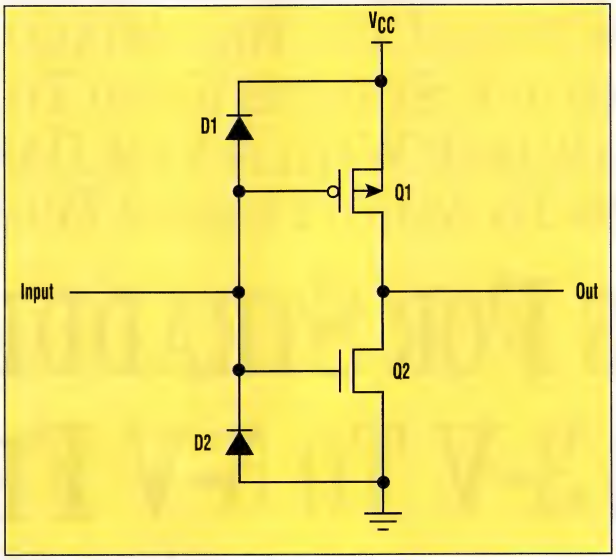
TABLE 1: LVTTL AND LVCMOS INPUT SPECIFICATIONS

Parameter	Test condition*	Min	Max
High-level input voltage (V_{IH})	$V_{out} \geq V_{OH}(\text{min})$ or $V_{out} \leq V_{OL}(\text{max})$	2.0 V	$V_{DD} + 0.3$ V
Low-level input voltage (V_{IL})		– 0.3 V	0.8 V
Input current (I_{in})	$V_{in} = 0$ or $V_{in} = V_{DD}$	– 5 µA	5 µA

*For conditions shown as 'min' or 'max', use the appropriate value shown in Tables 2 and 3.
3-V nominal supply: $V_{DD}(\text{min}) = 2.7$ V and $V_{DD}(\text{max}) = 3.6$ V
3.3-V nominal supply: $V_{DD}(\text{min}) = 3.0$ V and $V_{DD}(\text{max}) = 3.6$ V

BRIAN C. MARTIN
Philips Semiconductors, 9201 Pan American Freeway, Mail Stop # 55, Albuquerque, NM 87113; (505) 822-7347.

article aims to tell system designers all they need to know in ten minutes of reading.



1. THE STANDARD 5-V CMOS input structure has two clamp diodes. Diodes D1 and D2 clamp overshoot and undershoot on the input, as well as provide ESD protection.

JEDEC set two basic interface standards for 3-V components: low-voltage TTL (LVTTL) and low-voltage CMOS (LVCMOS). These specifications are intentionally very loose, and just about all 3-V components currently available satisfy both of them *(Tables 1, 2, and 3)*. It's interesting to note that while the two standards are very similar, their objectives are different. The LVTTL specifications are intended to provide input and output logic levels that are compatible with standard 5-V TTL. On the other hand, the LVCMOS specifications are set up so that standard 5-V CMOS designs can be used at 3.3-V, and vice versa. That way, IC manufacturers can develop output macros that function for either supply, and they can recharacterize existing 5-V CMOS parts as 3-V LVCMOS. Neither specification is intended to guarantee fully 5-V compatible components.

When mixing 3- and 5-V systems, two things commonly go wrong: data isn't properly transferred between the two systems, and current flows directly from the 5-V supply to the 3-V supply. While the first problem is relatively obvious, the second is not. Current flow from the 5-V supply into the 3-V supply should be avoided if possible. At best, it simply wastes power. At worst, it can damage the 3-V supply, burn out the path conducting it, or overheat the system. Any designer willing to live with such current should carefully evaluate any reliability issues.

There are three basic configurations when mixing 3- and 5-V components, each with its own design considerations: 5-V outputs driving 3-V inputs, 3-V outputs driving 5-V inputs, and both 5- and 3-V outputs sharing a common bus.

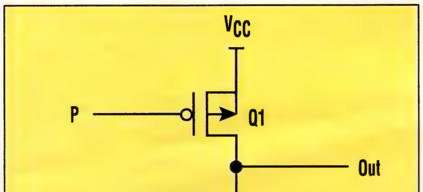
Table 1 shows the JEDEC input specifications for both low-voltage TTL and low-voltage CMOS. At first glance, it's apparent that both 5-V TTL and 5-V CMOS generate valid logic-low and logic-high levels for the low-voltage inputs. The only problem might be the V_{IH}(max) specification, which doesn't allow the input voltage to exceed the 3-V supply voltage by more than three-tenths of a volt. According to this specification, LVTTL and LVCMOS couldn't be driven by 5-V rail-to-rail CMOS. Even 5-V TTL becomes doubtful.

So, why this V_{IH} specification in the first place, and what can be done about it? A few 3-V ICs have such small device geometries that they simply can't tolerate potentials much higher than 3 V. Generally, it's not a good idea to drive such a part with a 5-V output. Fortunately, these parts are still rare (usually limited to certain microprocessors and DRAMs), and the V_{IH}(max) exists mainly because of the typical 5-V CMOS input structure *(Fig. 1)*.

Diodes D1 and D2 clamp overshoot and undershoot on the input, as well as provide ESD protection. Because many manufacturers made the quick jump into the 3-V market by simply recharacterizing their 5-V CMOS, many 3-V parts have the same input structure as shown in Figure 1. Obviously, if a 5-V part were to pull such an input 0.7 V above the 3-V V_{CC}, current would flow from the 5-V to the 3-V supply. Because these clamp diodes are designed to handle large surges, the magnitude of the current flow would be limited only by the drive capability of the 5-V output. JEDEC, being aware of this potential problem, included the V_{IH}(max) parameter in its specification.

Knowing the origin of the V_{IH} specification, designers can decide whether to drive their 3-V inputs with TTL outputs. If the 3-V supply were carefully regulated at 3.3 V and the static TTL-output level never rose above 3.7 V, then the input clamping diode would only turn on to clamp overshoot. In this case, there may be no issue. However, be aware that some TTL-compatible outputs pull higher than expected. For example, some 74ABTxxxx parts pull within a single diode drop of their 5-V supply. Consequently, 3-V inputs with diodes to V_{CC} should not be considered 5-V-compatible (not even with 5-V TTL) and should not (in general) be driven by 5-V components.

Fortunately, 3-V parts with 5-V compatible inputs are easy to find. Many manufacturers use alternative ESD protections to produce low-voltage CMOS inputs without the clamping diode D1 to V_{CC}. Good examples of such products include the 74LVCxxxx and 74LVTxxxx logic



P	N	Out
L	L	H
L	H	Not allowed
H	L	Z
H	H	L

2. A SIMPLIFIED CMOS-output structure helps show where current flow is going when the potential on the bus exceeds the potential of the 3-V power supply by 0.7 V or thereabout.

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TABLE 2: LVTTL OUTPUT SPECIFICATIONS

Parameter	Test condition	Min	Max
High-level output voltage (V_{OH})	V_{DD} = min, I_{OH} = – 2 mA	2.4 V	
Low-level output voltage (V_{OL})	V_{DD} = min, I_{OH} = – 2 mA		0.4 V
3.3-V nominal supply: V_{DD}(min) = 3.0 V and V_{DD}(max) = 3.6 V			

families from Philips Semiconductors. The inputs of these parts can be driven directly by either 5-V CMOS or TTL without any complications, and they should be easily identifiable by their product specifications.

One note of caution: Never mistake I/O pins for input pins. For example, say a designer wanted to use a 3-V PLD for a state machine that interprets fourteen 5-V inputs and generates four 3-V outputs. The designer finds a 3-V 22V10 without diode clamps to V_{CC}, hooks everything up, and discovers current flowing into two of the 14 inputs in the high state. A 22V10 contains 12 pure inputs and 10 I/O pins, two of which have been configured as inputs. Most I/O structures consist of an input structure and an output structure in parallel, and depending on the configuration, one or the other would be disabled. The output structure would be the problem in this case. In other words, the designer isn't just driving a 3-V input with a 5-V output, but a 3-V output as well. Thus, the situation would fall under the category of 3-V and 5-V outputs on a common bus.

Driving a 5-V TTL input with a 3-V output is extremely simple. As Tables 2 and 3 illustrate, the output-voltage levels of both LVTTL and LVCMOS drive TTL inputs nicely. In fact, there's even some margin because most available LVTTL and LVCMOS parts drive rail-to-rail. There should be no complications.

Driving a 5-V CMOS input with a 3-V output, on the other hand, is a major headache. By the way, 5-V CMOS doesn't mean TTL-compatible CMOS, but pure rail-to-rail CMOS. Ideally, the input threshold on a 5-V CMOS part is 50% of V_{DD}. Because V_{DD} varies between 4.5 and 5.5 V on 5-V systems, the output of the 3-V part would have to pull above 50% of 5.5 V for a guaranteed high. This is something that neither LVTTL nor LVCMOS (for V_{CC} = 2.7 V) is guaranteed to do. However, remembering the remark that most 3-V parts actually pull rail-to-rail, some designers might think that by lowering the 5-V supply to the lower half of its range and raising the 3-V supply to the upper half of its range, they could get things to work out. For anyone tempted to try this, let me throw out a few words of advice:

1. The actual 5-V input threshold can vary dramatically from part to part because of design differences between vendors and even process variations between lots. Consequently, the actual input threshold could range as high as 3.6 V.
2. Even if the 5-V input thresholds were low enough to be in range, the 3-V parts still couldn't give much margin against noise.
3. Assuming reasonable thresholds and adequate noise margin, the skew in propagation between low-to-high and high-to-low transitions through the 5-V part would be very large.
4. Because the input voltage would be around 3 V, both the NMOS and PMOS devices in the 5-V CMOS input would be partially on, thereby allowing current to flow directly from V_{DD} to ground—a waste of power.

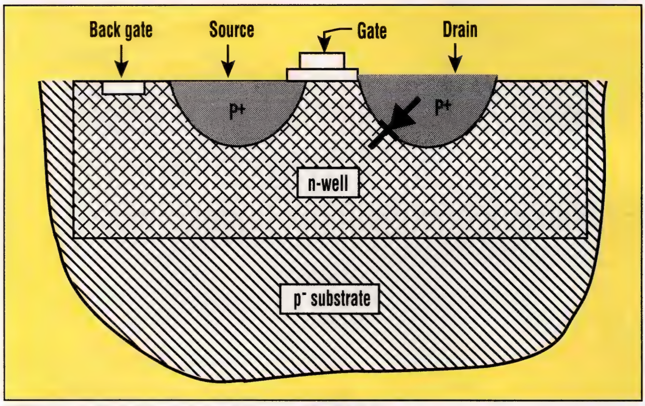
In general, it's not a good idea to drive 5-V CMOS with 3-V outputs.

Needless to say, there are always those persistent few who will find a way, regardless of how messy. For example, one suggestion I've heard is to connect a discrete pull-up resistor to the 5-V supply on the output of the 3-V part. The point of this configuration is to have the pull-up resistor pull the node higher in the high state. By itself, this really isn't a solution. Most available LVTTL and LVCMOS parts use PMOS devices in their pull-ups, which means they would contest with the pull-up resistor. In other words, the pull-up resistor couldn't pull the node that much higher without the PMOS dumping large currents into the 3-V supply.

The next temptation would probably be to place a diode in series with the V_{CC} pin. This would allow the pull-up resistor to pull all the way to the 5-V supply potential. However, the 3-V part's V_{OH} would then be lowered by a diode drop, making low-to-high transition speed rely even more on the pull-up resistor. If the pull-up resistor were small enough to guarantee a decent low-to-high speed, it would also be small enough to cause large static currents whenever the 3-V output pulled low.

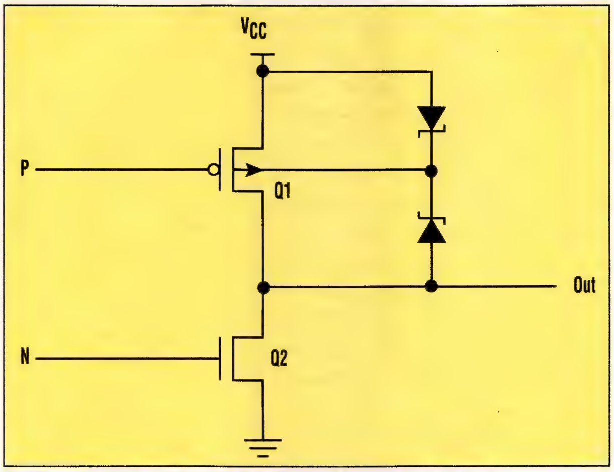
Furthermore, placing a diode in series with a component's supply pin can lead to some interesting side effects. For example, when the pull-up resistor takes the outputs to 5 V in the high state, it also pulls the component's internal power lines to 5 V through the output PMOS device. Among other things, this would radically raise the 3-V component's input thresholds. Although somebody somewhere has undoubtedly coerced some sort of arrangement to work, I'll re-iterate that it's not a good idea to drive 5-V CMOS inputs with 3-V outputs.

Many manufacturers offer CMOS translator chips as a solution to this problem. These chips have separate power supply pins for each side of the chip—the 3-V half interfaces to the 3-V system and the 5-V half inter-



3. THIS CROSS-SECTIONAL view of a PMOS device shows the large parasitic p-n diode from the drain to the back gate of Q1 that occurs in the circuit in Fig. 2.

faces with the 5-V system (the translation being performed on chip). Hitachi and IDT offer simple bus transceivers with this configuration. Other companies, such as Motorola, have programmable gate arrays and ASICs with architectures to perform this same translation. For pure CMOS, I think using a translator chip is the best solution. On the other hand, circuit cards using these chips require routing of both supplies and are no longer compatible with either a simple 3-V or simple 5-V system.



4. TWO SCHOTTKY DIODES CAN BE used to ensure that the parasitic p-n diode in Fig. 3 won't become forward-biased when the bus is taken higher than the 3-V V_{CC}. The two diodes hold Q1's back gate within a Schottky of V_{CC} or the output, whichever is greater.

In many situations, designers may want to have both 3-V and 5-V components sharing a common bus. At first glance, this may seem the same as combining the two situations discussed before. However, there's one difference: 5-V outputs are now driving 3-V outputs. This difference is significant enough that anyone who faithfully follows the trade journals is probably convinced that 3- and 5-V parts can't share a common bus. Untrue! Mixed 3- and 5-V TTL buses can be the best solution, but the appropriate 3-V components must be used.

Consider linking a 3-V memory card with a 5-V TTL backplane. Rather than designing a considerable amount of parallel circuitry and excess multiplexing, a designer may prefer to drop the card directly into the same bus as the others. The memory card would probably use a typical 3-V CMOS bus interface chip. Because most 3-V bus interface chips satisfy both LVTTL and LVCMOS specifications, it would have no problem generating valid TTL signals. The problem comes when the designer tries to three-state the 3-V part when a 5-V part is pulling the bus high. If the potential on the bus exceeds the potential of the 3-V power supply by 0.7 V or so, the designer will notice significant current flow into the output of the 3-V part even though it should be three-stated.

A simplified CMOS-output structure helps show where this current is going *(Fig. 2)*. To put the part in three-state, signal P at the gate of the PMOS Q1 and signal N at the gate of the NMOS Q2 are at V_{CC} and ground, respectively, keeping each gate off. Consider what happens, however, when the potential at the output exceeds V_{CC}. Because the source of a PMOS device is the conducting terminal connected to the higher potential, the output becomes Q1's source. If the output potential exceeds V_{CC} by a PMOS threshold or so, Q1 is no longer completely off. For example, with a V_{CC} of 3 V and an output potential of 4.3 V, Q1's gate-to-source voltage would be –1.3 V, and current would flow from the output to V_{CC}.

A much bigger problem exists, though. What the circuit model in Figure 2 doesn't show is the large parasitic p-n diode from the drain to the back gate of Q1. A cross-sectional view of a simplified PMOS device on silicon shows where this diode originates *(Fig. 3)*. The p-type source and drain sit in an n-type well called the back gate. The back gate is usually tied directly to V_{CC} so that this p-n junction doesn't become forward-biased. However, when the voltage at the output of a CMOS part exceeds V_{CC} by 0.7 V or so, this parasitic diode turns on directly to V_{CC}. The size of this diode scales directly with the size of the PMOS. In the case of a CMOS output driver, the diode would be large and the current's magnitude can be tremendous.

The situation is similar to the input clamp diodes to V_{CC} discussed earlier, except that now the outputs are the issue. As stated earlier, most 5-V TTL parts pull within two diode drops (approximately 1.4 V) of their power supply. As long as these are the only 5-V parts on the bus, and as long as the 5-V supply is less than 2 V greater than the 3-V supply, there shouldn't be much trouble. However, if the bus is taken any higher, or if the difference in power-supply potentials approaches 2 V, tremendous current will flow from the 5-V to the 3-V power supply. Because many systems are modular in nature, designers can rarely guarantee these conditions. Thus, the standard CMOS output should generally be considered incompatible with a 5-V bus.

To satisfy the LVTTL and LVCMOS V_{OH} output specifications, essentially all 3-V parts will require PMOS devices in their outputs. However, biCMOS processes give circuit designers the essential element needed to create 3-V parts with completely 5-V compatible outputs—the Schottky diode. The biCMOS 74LVTxxxx family from Philips Semiconductors demonstrates how Schottky diodes can be used to successfully three-state a 3-V output in the face of a 5-V signal.

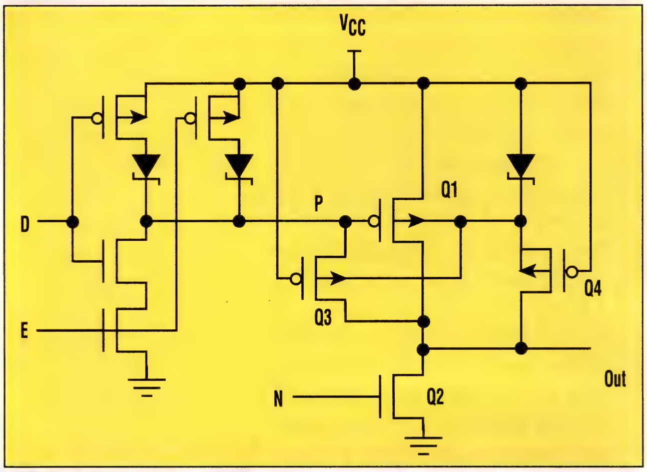
Two Schottky diodes can be employed to ensure that the parasitic p-n diode discussed earlier won't become forward-biased when the bus is taken higher than the 3-V V_{CC} *(Fig. 4)*. In this manner, the back gate is always held a Schottky below either

TABLE 3: LVCMOS OUTPUT SPECIFICATIONS

Parameter	Test condition	Min	Max
High-level output voltage (V_{OH})	V_{DD} = min, I_{OH} = – 100 µA	V_{DD} – 0.2 V	
Low-level output voltage (V_{OL})	V_{DD} = min, I_{OH} = – 100 µA		0.2 V
3-V nominal supply: V_{DD}(min) = 2.7 V and V_{DD}(max) = 3.6 V 3.3-V nominal supply: V_{DD}(min) = 3.0 V and V_{DD}(max) = 3.6 V			

V_{CC} or the output, whichever is greater, and there's no direct current from the output to the 3-V V_{CC} (note: p-n diodes can't be used for this due to the risk of latch-up).

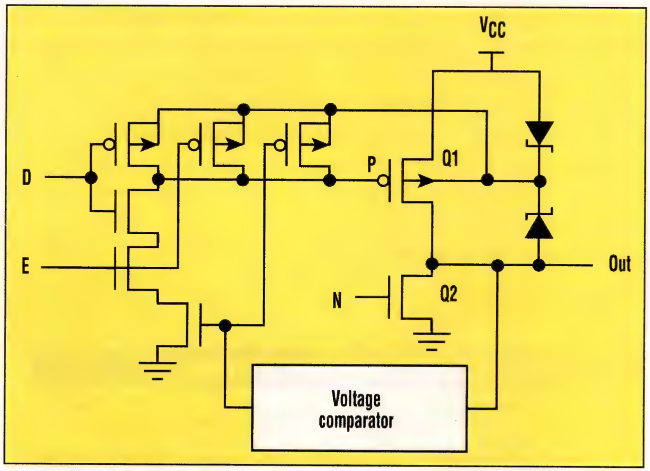
One biCMOS technique that's currently used can successfully three-state a 3-V output on a 5-V bus *(Fig. 5)*. The signals D (data) and E (enable) are NANDed together to drive node P at the gate of Q1. Note the Schottky diodes in the drain of each PMOS of the NAND. When either D or E go low, node P is pulled up to V_{CC} minus a Schottky diode drop. As long as the Schottky diode drop is lower than the threshold of the PMOS device, Q1 will be almost entirely off. The PMOS device Q3 is completely off as long as the output is V_{CC} or lower. But if the output voltage is taken more than a PMOS threshold above V_{CC}, Q3 will begin to turn on and charge node P up to the output voltage. Because Q3 charges P to the output potential, it ensures Q1 remains off when a 5-V component pulls the bus high. When this happens, the Schottky diodes in the PMOS-device sources in the NAND are necessary to block current from the higher potential at P to the lower potential at V_{CC}. Q4 performs the same function as Q3, except that it pulls up the back gate of Q1.



5. THIS 3-V OUTPUT circuitry can be three-stated in the face of a 5-V signal.

Apparently, many systems are designed with the notion that high is high and low is low, and therefore any number of parts should be able to pull a bus high or low at the same time as long as they all pull the bus the same way. Needless to say, this no longer holds true when mixing 5- and 3-V parts on the same bus. If 5- and 3-V CMOS parts both attempt to pull a bus high simultaneously, for example, the result is virtually a short of the positive terminals of the 5- and 3-V supplies. Although it's tempting to disregard this problem as sloppy system design, many new systems are often upgrades of ones that may already have this problem.

Philips has expanded the 5-V compatibility of its 74LVTxxx family to also protect against high contention *(Fig. 6)*. The basic technique is patent pending. In this case, the NAND gate driving node P has three inputs instead of two: D (data) and E (enable) as before, plus a third input coming from the voltage comparator. The voltage comparator's output is usually high, but goes low when the potential on the output exceeds V_{CC}. The sources of each PMOS device in the NAND are connected to the same node as the back gate of Q1—that is, a Schottky diode drop down from either V_{CC} or the output, whichever is at a higher potential. This technique limits positive I_{OH} currents to less than 100 µA and positive I_{OZ} currents to less than 20 µA when the output is taken above V_{CC}. Neither Fig. 5 nor Fig. 6 shows the complete output structures of Philips Semiconductors' 74LVTxxx products, but is meant to illustrate the basic principles behind them.



6. HIGH CONTENTION can be protected against by using Philips' 3-V-to-5-V compatible output circuitry. The basic technique employed in its 74LVTxxx family is patent pending.

So far, I've talked exclusively about mixing 5-V and 3-V systems. However, the issues surrounding input clamping diodes and output PMOS devices are relevant any time the potential at an IC's pin is greater than V_{CC}. A case of this occurs when logic signals are applied to an integrated circuit that's not powered up, such as during power-down or live insertion.

I use the term power-down to refer to intentionally powering down segments of circuitry in an active system to conserve power. Moving from a 5-V to a 3-V power supply saves considerable power, but many designers are discovering that temporarily powering down idle circuitry saves even more. Live insertion pertains to inserting a computer card into an active bus.

The problem in both of these conditions is that at some point inactive circuitry meets active circuitry. In the case of power-down, V_{CC} is usually held at ground. If the circuit of Fig. 1 has a logic high signal applied to either input or output, that signal would be clamped to ground through D1 or the parasitic diode inherent in Q1. Not only would this defeat the objective of saving power, but the data would be lost. In the case of live insertion, V_{CC} might still be coming up on the board when the bus interface makes connection. If the board's V_{CC} hasn't reached a sufficient level, input or output circuits similar to Fig. 1 would trash high signals on the bus.

Problems aside, power-down and live insertion are becoming very common due to increasing power consciousness and modularity. However, those obstacles do have a number of possible solutions. For example, special power-down architectures have been defined, usually around microprocessors. Designers also can achieve power-down by using components without input clamps to V_{CC} and implementing separate paths for data traveling in opposite directions. In this way, transceivers (which use I/O pins) can be avoided, powered-down inputs would present a high impedance, and no component with outputs tied directly to a bus would be powered down. For live insertion, many new specifications (for example, PCMCIA and VME64) include connectors with longer V_{CC} and ground pins so that a circuit card gets powered up before its bus interface makes connection.

Note, though, that the circuits in Figs. 5 and 6 address the problems of power-down and live insertion in the same way they handle 3-V-to-5-V interfacing, or any other situation in which the output is at a higher potential than V_{CC}. If an IC containing the circuit in Fig. 5 were completely powered down and a high voltage applied to the output, Q3 and Q4 would pull up both the gate and back gate of Q1. However, while this IC is powering up or down, it would be important to guarantee that either signal D or E was held low so that the NMOS stack doesn't simultaneously attempt to pull down the gate of Q1. On a simple logic transceiver, this could be accomplished by simply deasserting the chip's output enable as the board is powering up or down. The circuit in Fig. 6, however, has no such requirement. Whenever the output potential exceeds V_{CC}, the voltage comparator passes a low signal to the three-input NAND gate, and the gate of Q1 is held high regardless of D and E. Consequently, the circuit of Fig. 6 should be ideal for power-down and live insertion.

As system designers make the gradual move from 5- to 3-V systems, time-to-market considerations will require a shotgun marriage of the two. Furthermore, the practices of live insertion and temporarily powering down unused circuitry are becoming prevalent. Because all of these cases can cause headaches, those designers familiar with the issues involved will certainly have an advantage over their unenlightened contemporaries. Hopefully this article has enough information so that the typical designer avoids having to reach for the nearest aspirin.☐

Brian C. Martin, a logic design engineer in Philip's Standard Products Group, holds a BSEE from Brigham Young University, Provo, Utah, and is currently pursuing an MSEE from University of New Mexico, Albuquerque.

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CIRCLE 521

4-BY-4 CROSSPOINT HANDLES 100 MHZ

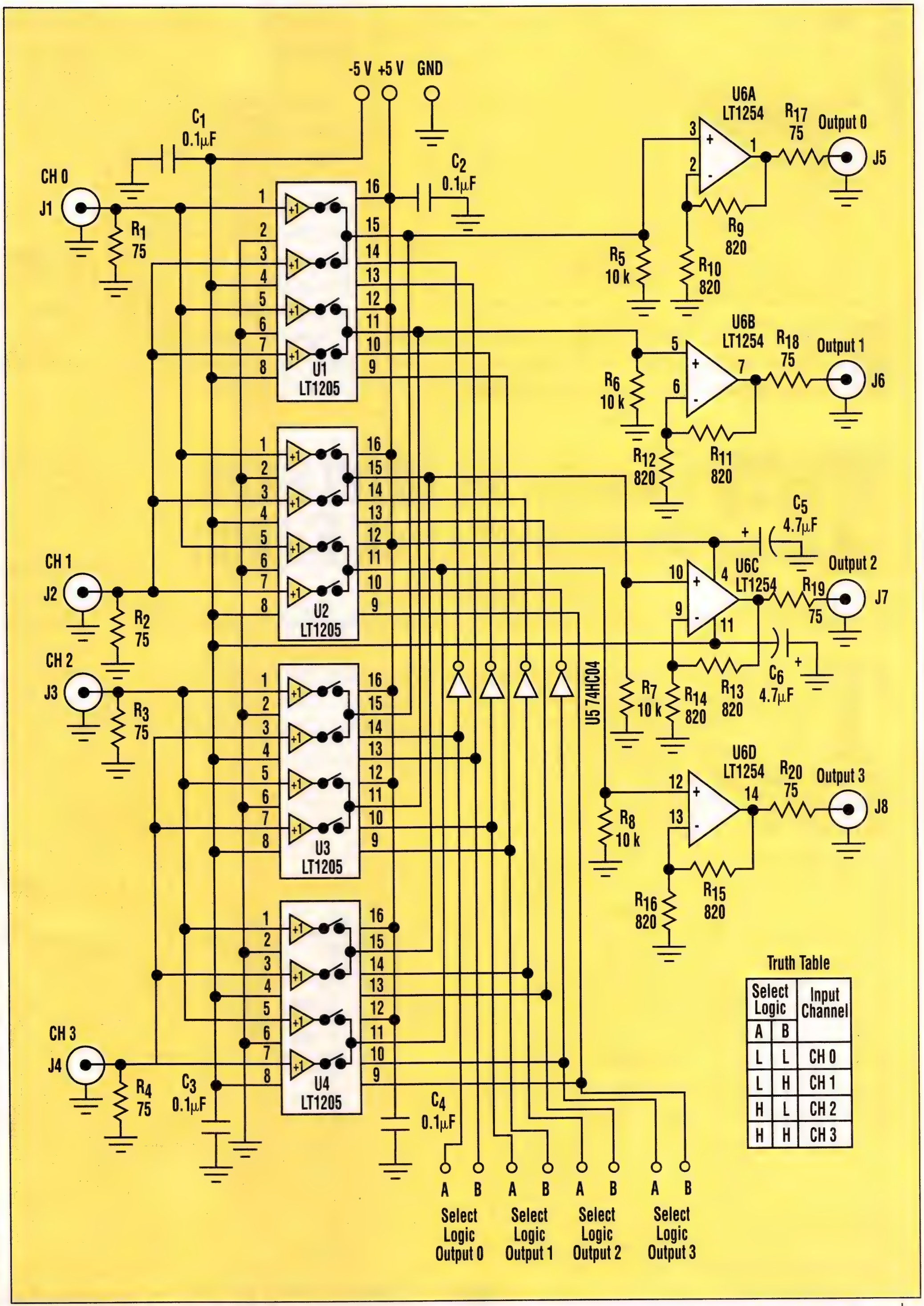
JOHN WRIGHT
Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487;
(408) 432-1900.

This compact, high-performance 4-by-4 crosspoint switch features a 100-MHz bandwidth and 85-dB crosstalk rejection. Four LT1205s are used to route any input to any or all outputs *(see Figure 1).* In addition, the complete crosspoint switch employs only six SO packages, and it occupies less than six square inches of pc-board space.

The LT1254 quad current-feedback amplifier serves as a cable driver with a gain of two. A 5-V supply is used to ensure that the LT1254's maximum 150°C junction temperature isn't exceeded in the SO package. With this supply voltage, the crosspoint switch can operate at 70°C ambient temperature and drive 2 V (peak or dc) onto a double-terminated 75-Ω video cable. The feedback resistors of these output amplifiers have been optimized for this supply voltage.

The –3-dB bandwidth of the crosspoint switch is over 100 MHz with only 0.8 dB of peaking. All-hostile crosstalk rejection is 85 dB at 10 MHz when a shorted input is routed to all outputs *(see Figure 2).* Keys to attaining this high rejection include:

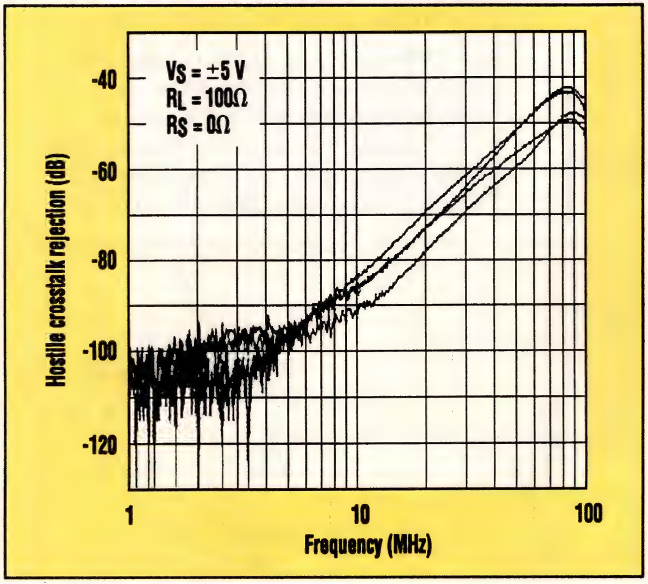
1. Mounting the feedback resistor for the surface-mounted LT1254 on the backside of the pc board.
2. Keeping the negative input traces of the LT1254 as short as possible.
3. Routing the V+ and V– for the LT1205s on the component (top) side and under the devices (that is, between the inputs and the outputs).
4. Using the pc board's backside as a solid ground plane, and connecting the LT1205 device grounds and by-



Truth Table

Select Logic A	Select Logic B	Input Channel
L	L	CH 0
L	H	CH 1
H	L	CH 2
H	H	CH 3

1. THIS COMPACT 4 by 4 crosspoint switch, which uses four LT1205s to route any input to any or all outputs, occupies less than six square inches of a pc board and has a 100-MHz bandwidth.



2. HOSTILE CROSSTALK rejection of the 4 by 4 crosspoint switch is 85 dB at 10 MHz. This curve shows the rejection characteristics of each of the four channels.

pass capacitors' ground as vias to the backside ground plane.

5. Surrounding the LT1205 output traces by ground plane and routing them away from the negative inputs of the other three LT1254s.

Each pair of logic inputs labeled "Select Logic Output" is used to select a particular output. The truth table helps in selecting the desired input, and is applied to each pair of logic inputs. For example, to route Channel 1 input to output 3, the fourth pair of logic inputs labeled "Select Logic Output 3" is coded A = Low and B = High. To route the Channel 3 input to all outputs, all eight logic inputs should be set high. Channel 3 is the default input with all logic inputs open. To shut off all channels, a pair of LT1259s can be substituted for the LT1254. The LT1259, a dual current-feedback amplifier, contains a shutdown pin that reduces the supply current to zero.☐

IFD WINNER

IFD Winner for December 16, 1993

R. Mark Stitt and Wally Meinel, Burr-Brown Corp., 6730 S. Tucson Blvd., Tucson, AZ 85076. Their idea: *"Photodiode-Amp Nulls Ambient Light."*

CIRCLE

522

CANCEL MULTIPLEXER ON-RESISTANCE ERROR

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290.

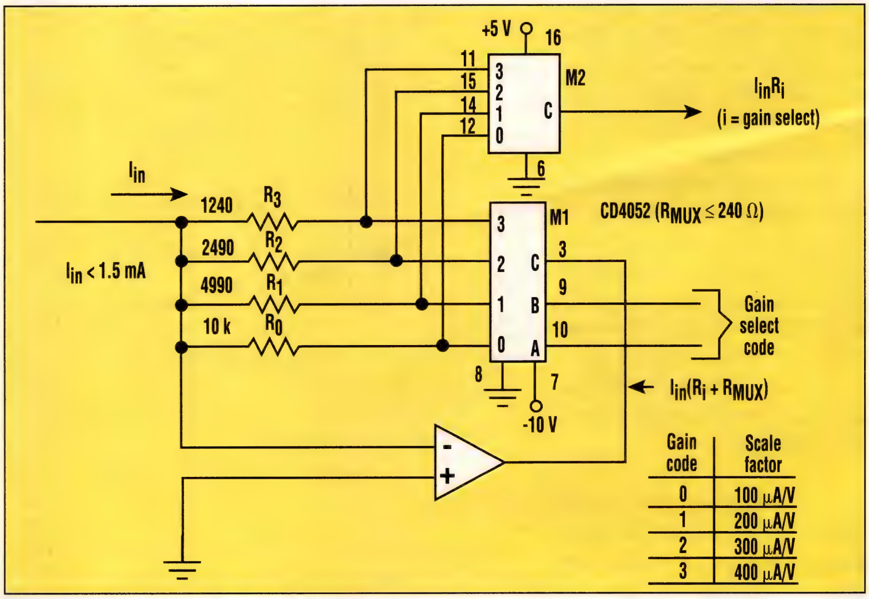
The classic inverting current-to-voltage converter is probably the simplest of all useful op-amp applications: a current-mode signal (I_{in}) is applied to an op amp's inverting input, which is converted to a voltage equal to $-I_{in}R_F$, where R_F is the feedback resistance. The situation gets messier, however, if digital selection of feedback-resistor values is needed.

The "mess" can be heavily attributed to the on-resistance of the multiplexer that selects the feedback resistors. Because this resistance is effectively in series with the selected feedback resistor, the magnitude of the converter's output voltage will be $I_{in}(R_F + R_{on})$ instead of the desired $I_{in}R_F$. R_{on} for popular multiplexers will range from tens to hundreds of ohms, and can thus cause unacceptable errors for feedback-resistor values in the range of 100 k and below.

A solution is to add a multiplexer (the dual CD4052's second half) *(see the figure)* that connects the output node to the selected feedback resistor's drive side. Thus, the R_{on} of the gain-select multiplexer is bypassed.

What results is a near-ideal transfer function of $-R_F$, limited only by resistor tolerance and amplifier error. At the same time, the R_{on} term causes the voltage at the op-amp output to err by as much as 20%.

One downside of the method is that it results in an output impedance dominated by the R_{on} of the extra multiplexer. However, this usually isn't a significant error source.☐



Gain code	Scale factor
0	100 µA/V
1	200 µA/V
2	300 µA/V
3	400 µA/V

ON-RESISTANCE ERROR in a current-to-voltage converter can be eliminated by adding another multiplexer that connects the output node to the drive side of the selected feedback resistor. Thus, the gain-select multiplexer's R_{on} is completely bypassed.

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CIRCLE 523

SIMPLE FULL-WAVE RECTIFIER

ALEXANDER L. BELOUSOV
3806 Fords Lane, No. 201, Baltimore, MD 21215; (410) 764-1605.

Using the circuit shown, you can build an extremely simple full-wave rectifier based on advanced rail-to-rail op amps in a single-supply mode *(see the figure)*.

The circuit operates as follows: When the input voltage is negative ($V_{in} < 0$), the voltage at point 2 is $V_2 = |V_{in}| \times (R_2/R_1) = |V_{in}| \times K_r$, where $K_r = R_2/R_1$ (the standard inverting amplifier gain equation). When $V_{in} > 0$, then $V_2 = |V_{in}| \times R_3/(R_1 + R_2 + R_3)$.

To provide the gain symmetry for both polarities, the relationship between R_1, R_2 and R_3 must be: $R_2/R_1 = R_3/(R_1 + R_2 + R_3)$. It can also be written as:

$$R_3 = R_2 \times (R_1 + R_2)/(R_1 - R_2)$$

$$= R_2 \times (1 + K_r)/(1 - K_r)$$

For example, if $K_r = 0.5$, the values of R_1, R_2, and R_3 will be those shown in the figure.

The unity gain of the entire circuit from input to output is obtained by adding a noninverting amplifier module with a gain of 2.

Several types of modern rail-to-rail op amps were tested. The main criteria was the accuracy of ac-to-dc conversion in the audio frequency range. The best results were obtained with the TLC2272ACP, a dual rail-to-rail op amp from Texas Instruments. The total error of ac-to-dc conversion for the sinusoidal waveform was less than 3% in a 10-Hz to 20-kHz range and less than 0.5% in the frequency range below 1 kHz. The circuit displayed similar results with the LMC6082 and LMC6482 dual op amps from National Semiconductor.

In the prototype circuit, a +5-V single power supply was used. This limits the input voltage to ($-2.5\text{ V} < V_{in} < 2.5\text{ V}$), or in other words, to half of the supply voltage. The maximum output voltage was also 2.5 V, but it can be increased to full scale (+5 V) simply by raising the output amplifier's gain to 4 (in the figure, the resistance of R_4 then will be 300 k). To increase the input voltage range, the supply voltage may be increased, or a voltage divider can be added.

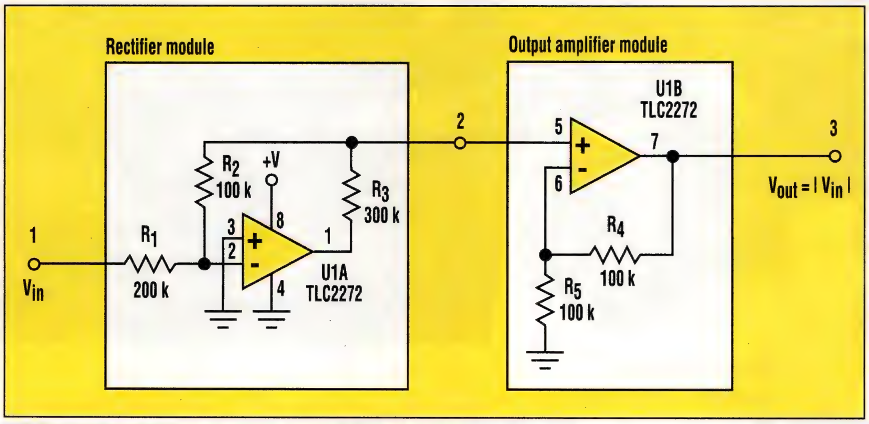
The equivalent input resistance (R_{eq}) of the rectifier module is different for different polarities of the input voltage:

$$R_{eq} = R_1 \text{ for } 0 > V_{in}, \text{ and}$$

$$R_{eq} = (R_1 + R_2 + R_3) \text{ for } V_{in} \geq 0$$

Consequently, the impedance of the signal source must be smaller than R_1 to prevent additional error and asymmetry of the waveforms.

To achieve high performance at reasonable cost, the best option is a low-cost resistive network with "ratio-matched" resistors, so that the absolute accuracy of the resistor values won't matter. A Murata-Erie resistive network such as type V, RSL7V104F, 100 k, or a TDK RHC series can be used in this circuit.☐



THIS SIMPLE FULL-WAVE RECTIFIER is based on advanced rail-to-rail op amps. To get both high performance and cost-effectiveness, it's best to use a low-cost resistive network with "ratio-matched" resistors.

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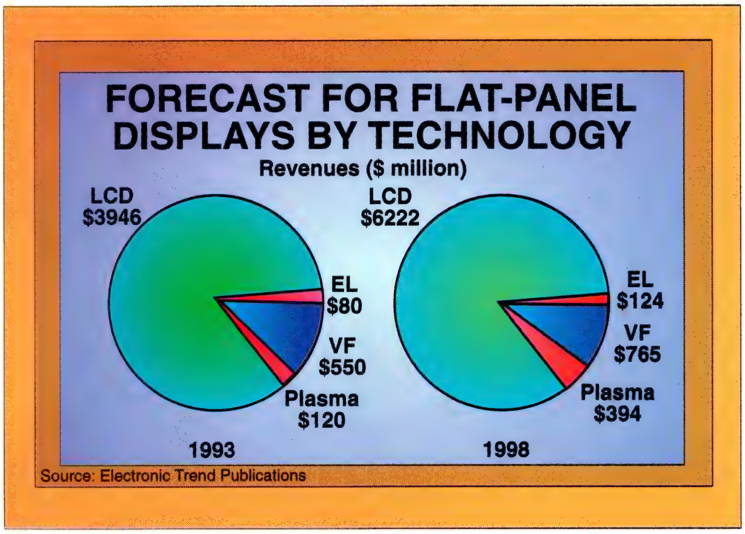
ELECTRONIC DESIGN QUICK LOOK

EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Flat-panel displays, which amounted to a $4.7 billion market last year, are forecast to be worth $7.6 billion by 1998, a 10.1% growth rate. That's the prediction of Electronic Trend Publications, a San Jose, Calif., market research company. Unit volume is expected to grow from 400 million units last year to 680 million in 1998, a growth rate of 11.3%. The leading technology is the liquid crystal display (LCD), which has evolved from simple character displays in watches and calculators to today's active matrix displays for high-end portable computers. This technology accounts for 84% of the display's revenues and 56% of the unit volume. Second in revenues and unit volume are vacuum fluorescent (VF) displays, which account for 44% of display volume. Because they are used in low-cost, simple instrument panel applications, their revenues account for just 11.7% of the market total.



Source: Electronic Trend Publications

TIPS ON INVESTING

Even for engineers, sorting through the many types of investment choices can be a big challenge. However, the process is easier if you can keep in mind general principles about how securities work and how they relate to one another. Here's a one time proven maxim: The longer you hold them, stocks usually perform better than bonds, money market funds, and other securities. Nonetheless, stocks tend to rise and fall more dramatically in any given month or year.

If you've ever owned a stock, you know something about stock-market cycles. Prices rise and fall as surely as tides surge and ebb. Generally, the stock market cycle and the economic cycle run the same pattern—but not at the same time.

Be aware that market cycle theory and reality are often different. Stock market cycles are like the weather—you can't predict exactly what's going to happen. The next bull market is not going to be just like the last one. Also, certain stocks buck the trend: Some perform poorly in bull markets, while others may climb in declining markets.

The key to balancing risk and reward is diversification. Spread your investable assets over several classes of stocks. Invest more in small company stocks if you are an aggressive investor, more in blue chips if you are conservative.

Many factors influence stock performances: the economy, interest rate movements, government actions (such as taxation, federal spending, as well as industry regulation), the returns available in the bond market and other alternative investments, as well as human emotion. Changing technology, the time of year, and emerging domestic and overseas markets also play important roles.

Before buying stocks, it's a good idea to check what experts are saying. Stock research generally takes two forms: fundamental analysis and technical analysis.

Keep in mind that while the past can help somewhat in forecasting the future of stocks, the winds of economic, political, and technological change blow in constantly changing patterns. Experts alter their opinions frequently. For example, throughout 1993 stocks generally increased. Now, some analysts say stocks are expensive and are warning of a significant drop in prices. Other experts believe stocks will continue to climb: They believe inflation will remain low and some interest rates will continue to fall, boosting stocks.

Gathering information is critical because in all market conditions there are good and bad performers. The more selective you are in buying stocks and the longer you hold them, the greater your rewards are likely to be. For more in-depth information about stock market evaluation, or to discuss how current events could affect specific stocks, speak with a qualified financial consultant.

For a free copy of "Where We Stand," a Smith Barney Shearson Publication, call (800) 631-2221 or write to Henry Wiesel c/o Smith Barney Shearson, P.O. Box 8729, Red Bank, NJ 07702. Henry Wiesel is a financial consultant, investment counselor, and qualified pension coordinator with Smith Barney Shearson. Wiesel invites questions and comments from Electronic Design readers.

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Ba

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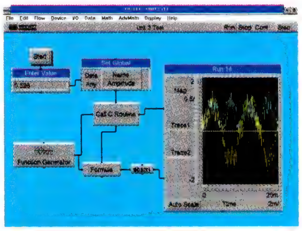
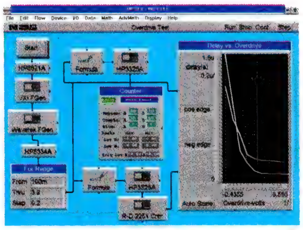


Standard language ties give you the flexibility to use existing code or create new C routines.



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CIRCLE 460

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EYE ON ISO 9000

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KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

Why does your organization need a new product development database? Fundamentally, the database explicitly addresses the person-hours necessary to develop and introduce a new product. When the introduction date is pulled in, the number of person-hours has to be effectively modulated through resource and functionality adjustments to meet product availability objectives. To get time, interactions with resources, functionality, and money must be managed— the effort's database enables the production of timely and accurate decisions.

Current management tools can explicitly address the modulation of person-hours within a project if you know how to use them for this purpose. Microsoft Project is a good one— most others can do the job also. These are PERT/CPM tools that represent each activity by the number of person-hours needed to complete it and they can total the person-hours required for the entire job. While these tools have the ability to model work, they can also be used in a non person-hour mode.

And in fact, most users I observe use the tools in the date-driven mode only. That is, start and finish dates for each piece of work are entered, but no information about the work hours necessary to do the task is furnished.

If you are working in this mode, give serious thought to making a behavioral transformation. These tools have to allow date-based activities (for example, fab and assembly throughput time), but this is not where their power lies. Use them without work and resource information and they become presentation managers. Put work and resource information in to use their full capability.

A simple example illustrates the difference between date-based and resource-based methods. In the former, a task's finish date is computed from its start date using a user-supplied duration figure—a task starting on 1/1/94 with a duration of 2 days finished on 1/3/94. Whereas a 16-person-hour task that starts on 1/1/94 completes on 1/3/94 only if a resource works on the task at an average rate of 8 hours per day.

Should a resource not be assigned, the task never completes. Or if it can be worked on at only 1 hour per day, then 16 working days go by before this segment of work completes. Or maybe two individuals could team up and finish the work in a day. In the latter method, duration is computed from resource commitments and task work content. Regular readers of the column should be familiar with background duration computation information. Building a project database that accommodates resource-driven, duration computation methods has significant payback.

In the resource-driven mode, all dates except today's date are computed—no dates are entered! In fact, after supplying task, work quantity, commitment, resource, and network information to construct the project's model, you enter only the remaining work on each task to maintain the database and thereby maintain your schedule. Should problems with time, resources, functionality, or money be observed, the database provides the structure needed to resolve the issues.

To realize your time goals, you have to effectively manage the area under the work versus time curve. A project database, resident in Microsoft Project or in a similar tool, facilitates this important endeavor during the execution phase of your project. But it is well to remember, for the database to work for you and not against you, it must be used in the duration computation mode!

"It's About Time!" a workshop of new-product development organization will be held at Santa Clara University's Executive Development Center on April 7, 1994. For information on attending the seminar, contact John Blumenson, the center's assistant director, at (408) 554-4521; fax -5143..

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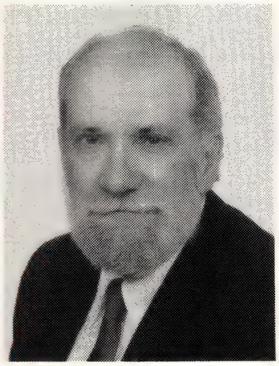
QUICKLOOK

MY VIEW

...About Intel Inside

BY FRANK J. BURGE
Director of Market Development for Electronic Design



Depending on where you sit, the *Intel Inside* campaign is either the most brilliantly conceived and executed marketing strategy in the history of the electronics industry or the worst—if you're an Intel competitor. More dollars have been spent by Intel and its PC co-marketers on the *Intel Inside* advertising campaign than on any other campaign in the semiconductor industry. (My friends on Wall Street keep reminding me that Intel is a computer company, not a semiconductor company.)

Intel started talking about an ingredient-branding strategy in 1988, and its agency studied the NutraSweet and Dolby approach to ingredient-brand development. It wasn't until July of 1991 that the program was funded and finally launched. The *Intel Inside* campaign was intended to fend off the Intel clones and slow what appeared at the time to be an inevitable erosion of market share. Now let's look at the numbers provided by Dataquest:

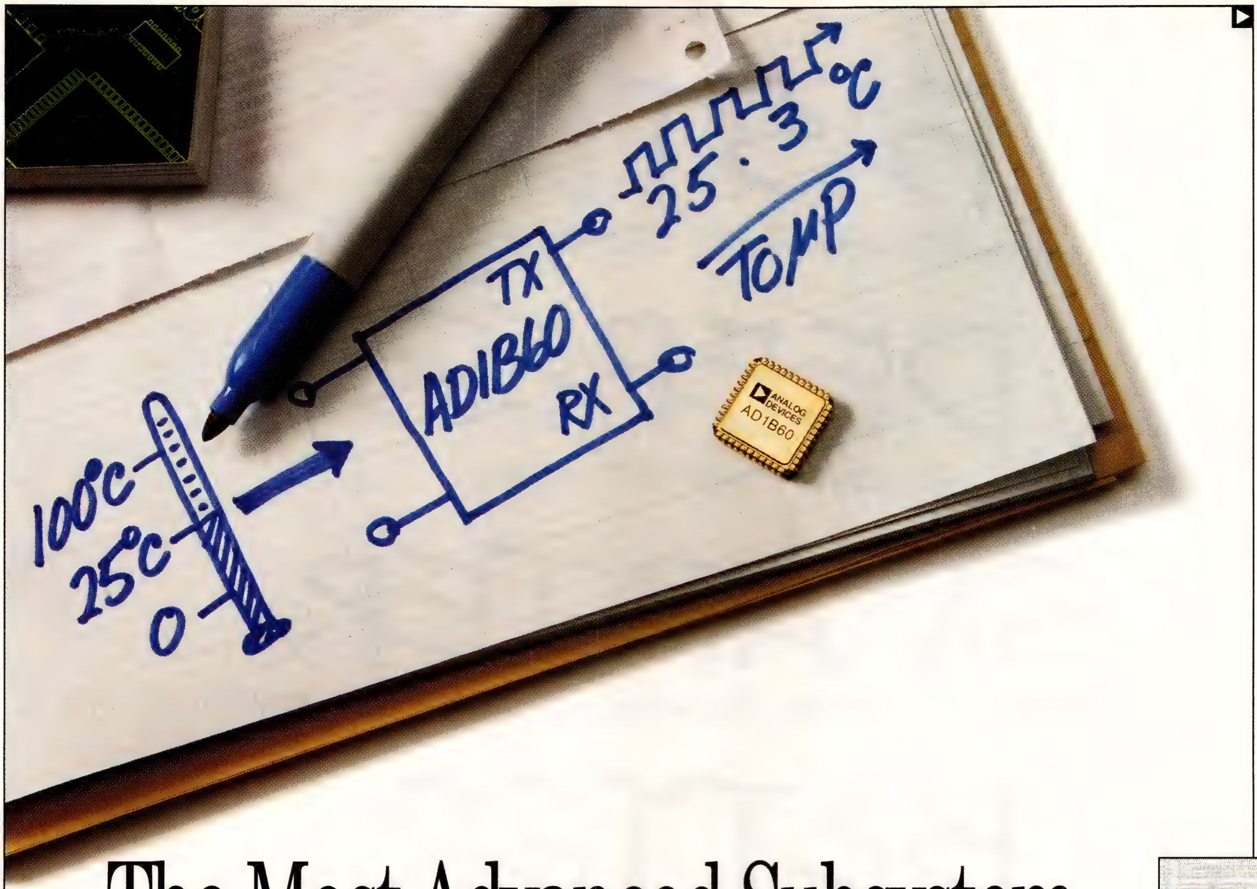
Microprocessor market

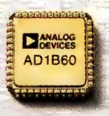
	1990	1991	1992	1993
($ billion):	$2.8	$3.9	$ 5.5	$8.6
Intel share:	64.5%	64.1%	68.8%	74.0%

Was the *Intel Inside* campaign a success? You bet—just look at the numbers for market growth and share growth since the campaign was launched in 1991. Were there other factors that influenced the uptick in Intel's market share? Of course, but it was the advertising that brought Intel's commitment into the living room and the board room. Brand-building in the consumer market takes deep pockets. In the 33 months since the launch of the campaign, Intel and its co-marketing PC partners have thrown the equivalent of over $400 million in advertising dollars at the market. In the consumer brand-building game, you need big bucks and lots of patience. Play for the long haul or stay home is the name of the game. How do the PC manufacturers feel about *Intel Inside*? All of them benefit from Intel's sharing the cost of their advertising. Since Intel is picking up a good chunk of the tab, it meant the PC players could do at least twice as much advertising with the same ad budget.

And with all that PC advertising being thrown at the market, PC unit shipments shot up. For the second-tier PC manufacturer, the *Intel Inside* logo on its PC gave it instant credibility. This co-branding strategy leveled the playing field and was reason enough to go with Intel rather than with a less costly alternative. But what happens if you're a top-of-the-charts PC player, let's say an IBM or Compaq. The *Intel Inside* logo makes it more difficult to differentiate your offering from the others, since the assumption is that all PCs with *Intel Inside* are equally good.

Does the co-branding strategy work against you? Maybe. But all that PC advertising being thrown at the end-user market drives up demand. And your slice of the bigger pie more than offsets any disadvantage. Now even the big guys use *Intel Inside* in their advertising. They're afraid not to. I've often heard that Intel is arrogant. Some suggest that Intel is a relentless competitor with a crush mentality—crush the competition in the marketplace and in the courts. Paranoid too. But one thing is also true: Intel is a great marketing company. And I am old enough to remember when Andy Grove pretended he couldn't even spell marketing.





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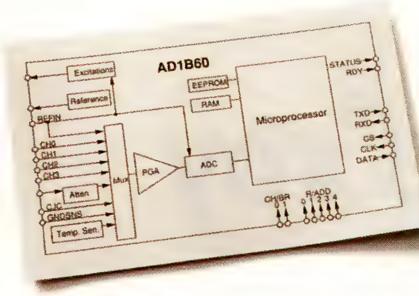

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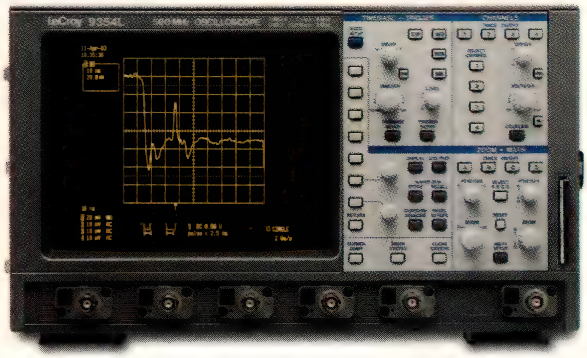

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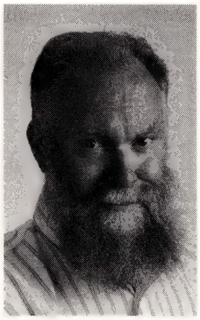
WHAT'S ALL THIS HOAX STUFF, ANYHOW?

As I warned you guys, April is a good time of year to write about hoaxes, and several people have sent me some neat ideas. But one guy asked, "Bob, what is the difference between a Hoax and an April Fool joke?" I told him that you can't tell from the way it starts out, but by the time you get to the end, a good April Fool joke should give you enough clues so you can start to smile. But if you're merely puzzled, or skeptical, that could be a hoax. Conversely, if the guy tops off his story with "and send money," that's a clue that it may be turning into fraud. But sometimes, the guy isn't aware that the situation is impossible—he has fooled himself badly, and may be unaware of the truth. So if you're just listening to the start of the story, *or the end*, you can't always tell.



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

As I mentioned earlier, some of the stories about Fuzzy Logic start out like an April Fool joke, but after you figure out that the guy is serious, then it's only just funny. However, we have seen some claims, such as "only with Fuzzy Logic can an elevator avoid lurching." That's more like self-deception. Or, "The Sendai train is 10% more efficient than a train without Fuzzy Logic, and runs faster, too." That's a *scream*!! (Details available on request.)

Back in October, I heard a good program about hoaxes on the radio and sent away for the *Encyclopedia of Hoaxes* that they mentioned on the show.[1] It really is a pretty good collection of Hoaxes, April Fool jokes that went too far, etc. But, unfortunately, it doesn't include any hoaxes in the field of electronics. So after I publish this column, I'll have to send a copy to the author so he can include some of the following stories about hoaxes in electronics.

Let me start out with the Tice Clock. This clock is a basic LED digital clock, substantially identical to a $30 clock sold by Radio Shack. But George Tice sells this for $270. He makes some very lavish claims that by plugging this clock into your audio amplifier's main 115-V power socket, the clock will make all your audio equipment sound much better—that is, if you have a "Golden Ear." However, if you can't hear any difference, then you're admitting that you don't have a Golden Ear—that you have only limited auditory capability to appreciate the BEST in audio.

Many reviewers for hi-fi magazines have agonized over this. A few think it's great—the reviewer can really *hear* the improvement. Others search for any plausible technical reason for improvement. One reviewer observed, "If Mr. Tice enclosed a Negative Ion Generator in his clock, maybe people really WOULD think the music sounds better." But he had to concede that there was NOT any ion generator in there. So, many people have come to the conclusion that this clock is (at best) a hoax.

They can't hear any difference, and there's nothing to measure. There's no subjective or objective reason to think that Tice's "clock" can make the music sound better. But it sure takes a lot of *brass* to make such claims.

On the other hand, some people think that painting a green magic marker line around the circumference of a CD makes it sound better. Some people think that putting a new part number on an old op amp makes it sound better. Some people think that dunking a 16-bit DAC in liquid nitrogen for a while makes *that* sound better. Maybe you can hear the difference. I can't.

Now, let me digress briefly. Let's say you have demonstration models of some good loudspeakers. How do you decide that type A is better than type B, or, that it's *different*? Mr. David L. Clark, Chief Engineer, DLC Designs, Farmington Hills, Mich., combined a set of relays and a random number generator to make an "ABX" tester. If you push the switch for A, the tester connects to the A speakers, or the A set of wires, or whatever. Then you can listen intently and decide that the sound you're listening to is the "A" sound.

If you hit B, you get channel B, and you listen to "the B sound". If you push X, you get a random selection and you jot down whether it's channel A or B. At the end of 10 tests, let's say that you have listed: A, B, A, B, B, B, A, A, A, B. Once that sequence is completed, the ABX box will tell you what it ACTUALLY connected. If you listed 8 out of 10 correctly, that's a lot better than just guessing—you probably did hear a difference. If it's 4 or 5, well.... who knows? In some cases, some people with really good ears can hear things that I cannot. In other cases, they're unable to tell. In yet other cases, they refuse to try because they don't like the test.

Still, when speaker cables of different types or characteristics are connected through an ABX box, some people with "really good ears" can hear the difference IF the wires have different amounts of inductance, capacitance, or resistance. It's generally admitted that no matter how exotic the materials or the construction techniques, if two sets of wires have the same R, L, and C, you can't tell them apart. Nobody can.

So you'll find that one guy wants to sell you 10 feet of speaker cable for $100; another guy claims his are a

PEASE PORRIDGE

LOT better, and they MUST be better *because* they cost $300 for 10 feet; and then a similar claim is made for a $480 cable. But if they all have the same R, L, and C—and each one spouts claims such as.... "superior imaging," "finer presence and less phase shift," etc., etc.—that strikes me as somewhere between fraud and hoax.

You can spend your money any way you want to. You can say that you hear a difference. But if I offer you an ABX test, you should not get mad at me and stalk out.

Some of my favorite "hoax" stories are just the claims that manufacturers of speaker cables tell about their wires. I really like the cable with "large-diameter wires to carry the low-frequency music, and small-diameter wires to carry the high-frequency music." (Of course, it's easy to compute that the skin effect of copper wire will make a 3° difference in the phase shift of the thin/fat wires at about 300 kHz. And, since the fat wires and the skinny wires are paralleled, you won't be able to see any significant difference in phase shift at 20 or 30 kHz.)

The other cable I'm impressed with is the stuff that has a conductive "insulation." When this cable's resistive losses match the capacitive and inductive attenuation and the conductive losses, and the phase shift is minimized, it should sound better.

Well, if it sounds better to *you*, go ahead and buy it. But, if it just sounds *different*, then maybe you do want to buy it—or maybe you don't. Maybe when you really turn up the volume, the conductive "insulator" will start to get hot??

Speaking of cables, my friend Tom said that his wife recently went to buy some new speakers at Circuit City. The salesman sold her some new speaker wires "because the old ones were probably worn out."

Additional amazing audio quasi-hoaxes:

(a) When you have line-level cables (with RCA-type phono jacks), the expensive cables sound *much better* than inexpensive ones.

(b) After you decide to specify the expensive cables, the ones with gold-plated jacks sound *much better* than the solder-plated ones.

(c) These cables have a preferred direction, and sound better when you connect them up in the preferred direction, with the arrows pointing *from* the tuner *toward* the amplifier.

(d) In addition, these cables sound better if they have been broken in, or *aged*, with a special ac signal forced through the cable.

(e) The best burn-in fixture for these audio cables uses *digital* signals to force current through the cables.

Needless to say, I've never heard of any one of these wonder cables being tested with an ABX box. Probably the "Golden Ear" person would object to the relays in the ABX box, as they would *corrupt* the signal. But maybe we could overcome those objections by using a digital burn-in circuit to burn in the ABX box....

The next area I'll mention briefly is the "vacuum tube sound." This isn't about a hoax, but rather a chameleon. It's well known that some audiophiles prefer audio amplifiers made with vacuum tubes. They claim that the ratio of 2nd-order harmonic distortion versus the 3rd-order is more pleasing with a good vacuum-tube amplifier. Maybe so. Myself, I've got a tin ear, not golden, so I'm not very picky. (Maybe I did too much chainsawing as a youth, or turned up the volume on Chuck Berry too many times.)

But Mr. Carver, an excellent designer of audio equipment, came up with a beautiful ploy: He took one of his low-distortion solid-state amplifiers, and added a circuit with a little bit of 2nd harmonic to make it "sound like" a vacuum-tube amplifier.

I'm not familiar with this amplifier's ABX comparisons, but I think it's a NEAT idea to make a chameleon amplifier like that. I think it's great to see if the Golden Ear guys can be fooled.

About 30 years ago, when transistors did not have much performance, a contest was run to make a small high-performance audio amplifier. The late Peter Lefferts won the prize, with a small (6-in. cube) block and heat fins. Inside were a couple of small (6L6GB?) tubes running hot but with good heat sinking. They were legal under the rules, and nobody else thought of doing that.

A friend told me about a promoter with this scheme: They had a conventional TV transmitter, and at the end of each cycle, just before the zero crossing, they would insert a brief pulse signal before the normal RF signal resumed. Then a specially designed receiver could detect those pulse signals and extract additional info. At 200 MHz, you could also get 200 Mbits/s, free, *without any increase* of the RF bandwidth.

Further, this excellent communication scheme was backed up with a U.S. Patent and a big development company formed by a guy named Gerdes. As soon as I heard this line, I got VERY suspicious. My friend promptly admitted, "Of course, after a big press conference where this great technology was announced to the world, several engineers confronted the inventor and insisted that any studies showing you could do that without requiring more bandwidth were obviously malarkey.

The development company folded up.... the promoter hasn't been seen since." Yes, *that* sounds like a hoax—or a marvelous example of self-delusion. These days, there are entirely too many cases where computer simulation leads an inventor to believe it will work....

Gunnar Englund of Gransbergsdal, Sweden, once proposed some filters for line power that would filter out any electric power generated with nuclear power. He figured he could sell lots of them to environmental fanatics, with the guarantee that the output power will not show any nuclear residues. But then he got nervous about prospects of a criminal record, even though his guarantee would surely hold up.

Here's another good hoax: Mr. H. told about a group of engineers at Northrup, who in the 1960s invented a "metric tensor sensor"—a meaningless non-invention with a melodious name. They even got a dummy patent application all drafted. Unfortunately, the senior manager signed it off and sent it to the Patent Office before anybody could explain. THEN they had some explaining to do....

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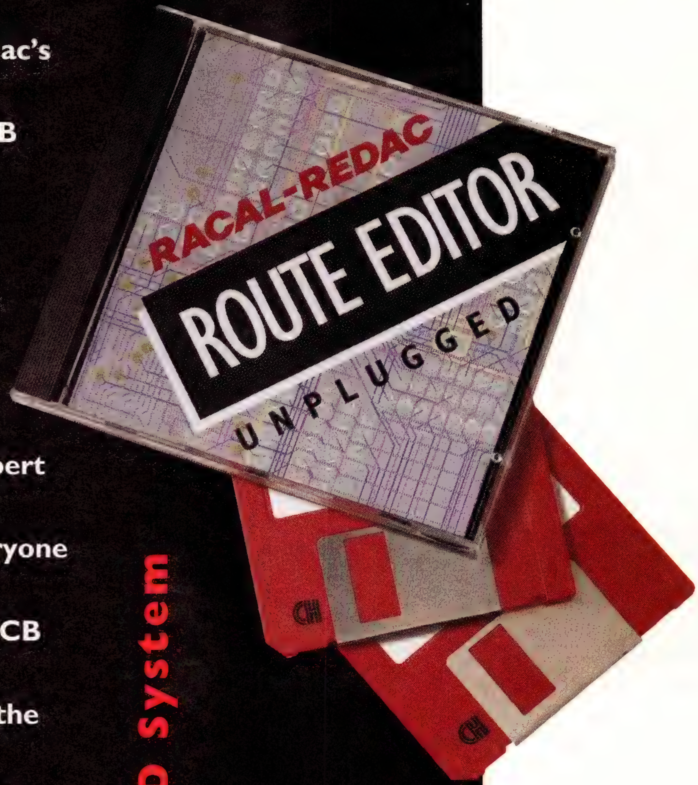

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PEASE PORRIDGE

An engineer from Basingstoke, England, sent in a classy little pamphlet produced by Motorola (U.K.) showing a new non-electromagnetic telephone that used the scientific principles embodied in 2 tin cans and a length of string. VERY nicely done. They even had a rare-earth barrier to protect the inner "Lirpaloof" fiber from fiber-eating locusts. Jolly good.

I have the Abstract of a U.S. Patent—a "Permanent-Magnet-Powered Motor".[2] Of course, the Patent Office won't approve of a patent on a perpetual-motion machine. But this one apparently snuck through.

Then there's Joe Newman who back in the 1980s invented a motor with *very* high efficiency.[3] It's so efficient, he claimed, that it puts out more power than it takes in. Further, he claimed that he could run a car with no more current than a transistor radio needs. Of course, when engineers saw him loading 1800 9-V batteries into the car, all stacked up in series, they realized that such a battery can indeed provide a full 1/3 horsepower when loaded with 16 mA. If you have a motor that's designed to work at that high voltage, you can indeed move a car at a slow speed for a short distance, as Mr. Newman has indeed demonstrated.

This was the guy who sued the Patent Office after they refused to patent his motor. When the NBS showed that his motor only *appeared* to put out more power than it took in, because he used an RMS voltmeter that couldn't accurately handle the low duty cycles and high harmonics that his motor ran on, he accused them of being incompetent at measuring things!! I've inquired about his progress at promoting his motor, and ran a literature search in our library, but nobody has heard *anything* from him for eight years.

In a scheme with similar ramifications, Norman Dean invented, back in 1956, a machine to "rectify centrifugal force."[4] First he set it up so that incoming rotary energy would cause some jerking motions. These could be synchronously detected by some clamps on a pole, which this apparatus could climb. Then Mr. Dean got the same basic scheme to run *without the pole*, just sitting in thin air! It could turn *energy* into *force*. He proved that it would do this because he could start it up on a bathroom scale, which would then start to read negative weight! Of course, nonlinearity of the scale mechanism was never considered. I first read about this in "*Analog Science Fiction*" magazine (which has nothing to do with analog circuitry), in which its masthead conceded that there wasn't necessarily a dot of truth in anything they published. Lovely!!

However, Mr. Dean proposed a large-scale demonstration. Get four of these "Dean Drives," one on each corner of a nuclear submarine, and—presto—you have a nice little space ship! "Why won't the Congress give a fair consideration of my invention?," he bleated.

My demonstration would be even more fun: get a couple of these "Dean Drives" running on the tips of a long rotor in a vacuum. You could put in 100 W, which would generate a certain number of ounces of force. Then, when you get the speed of the rotor up high enough, that few ounces of force would generate more power than the input power—thus, a perpetual-motion machine. Needless to say, this machine generated a LOT of controversy and head-scratching in its day.

Let's mention computers (some people have suggested that almost any use of a digital computer can be considered a hoax....). How fast can a computer display write? One well-known computer benchmarking program yields a result called a "Winmark." Part of the test originally consisted of repeatedly writing to the display: "The quick brown fox jumped over the lazy dog." However, some bright young guy figured out that if he set up a detector for that phrase, he could then shift into a hot-rod mode that couldn't handle anything else, but it could display *that* phrase *really fast*. His Winmark rating was much superior to anything else in his price range, until the trick was discovered. Then, every time a new task was set up, detectors would be told to search for the phrase and go into fast graphics mode. I think they finally gave up on that.

But, that's exactly like the Corvettes that have come out over the last couple years: If you start out moderately in first gear and try to shift up between 16 and 20 mph, a computer predicts that you must be trying to do an EPA test, locking out gears 2 and 3 and forcing you to shift to 4th gear. With this ruse, passing the EPA tests is easy. If you want to defeat this lockout, just wind it out to 25 mph, and then you can shift into any gear you want, because the computer knows you're not an EPA guy.

A couple of people told me about the young fellow who found a way to get much faster results in general-purpose computing by just adding a capacitor to the main board. Everybody was impressed with his excellent Whetstones! It took several days before some guy with a stopwatch realized that it didn't complete the task any faster—it just slowed down the clock for the task timer. The guy who had made a "lucky guess" did apologize—he really didn't know how he was being fooled.

Bob Dobkin was at National in 1975 when he invented a Darkness Emitting Arsenide Diode. This had many features—light output never fell off with time, and they were cheap due to high yield. Just check the acronym. Then in 1979, Dobkin "invented" a BD-1, a Battery-Discharger circuit. You manufacture this by taking a TO-3 regulator that's dead, and cutting off both pins. Then the resistance from one bolt-hole to the other is about 0.9 mΩ, and thus can be used to carry hundreds of amperes to discharge batteries, etc.... He got a good paragraph write-up in the April 1 issue of an electronics magazine. We all smiled at that one.

Then a few days later, I ran into Roy Essex, the marketing manager for power regulators. Roy was in a grouchy mood. I asked him why. He rambled on that a customer had called several times to get more information on some absurd Battery-Discharger chip, and he wasn't able to get any information about it, and the customer was getting madder and madder, and if there was any such chip, *he* should know about it, but he had no idea what the customer was talking about....

I replied, "Roy, did he call that

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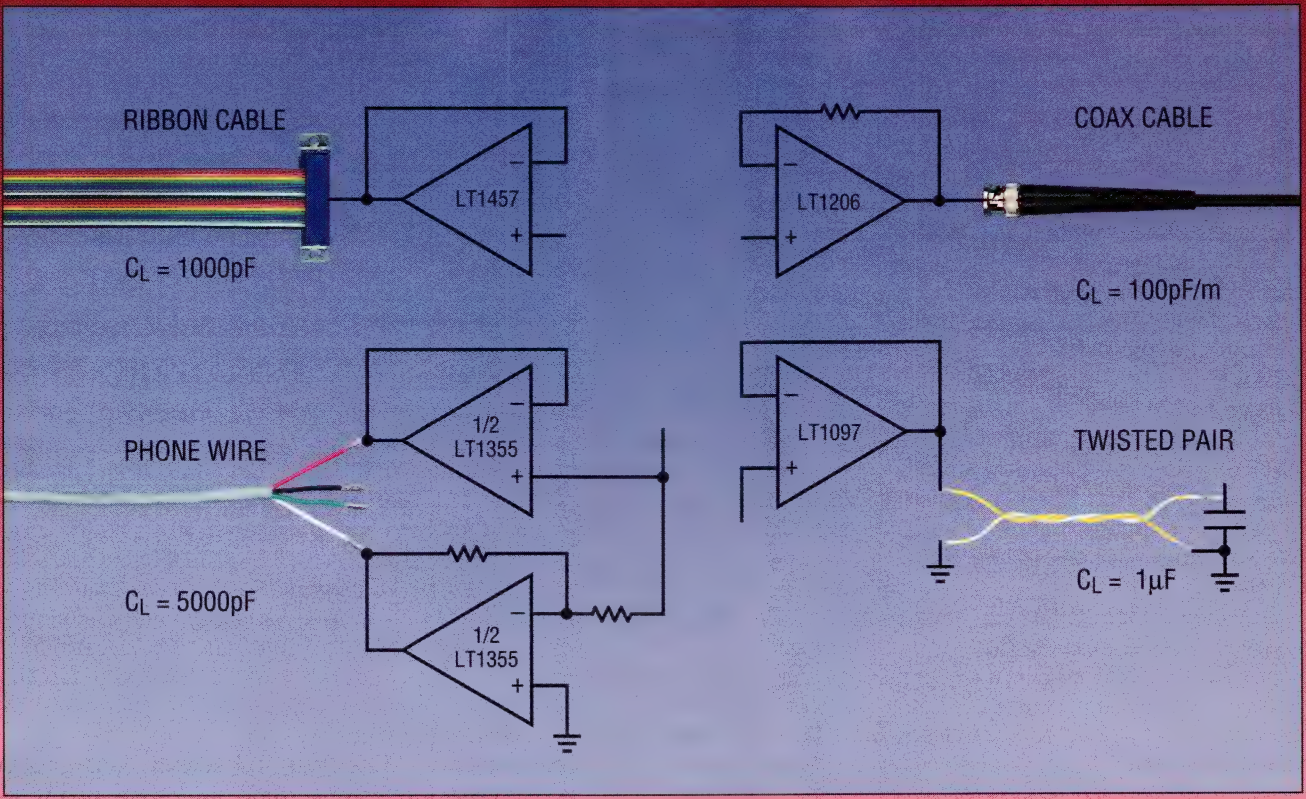

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LT1152	10µV	100pA	4mA	1MHz	1V/µs
LT1206	10mV	5µA	250mA	60MHz	900V/µs
LT1220	1.0mV	300nA	24mA	45MHz	250V/µs
LT1224*	2.0mV	8µA	24mA	45MHz	400V/µs
LT1354*	800µV	300nA	30mA	12MHz	400V/µs
LT1357*	600µV	500nA	30mA	25MHz	600V/µs
LT1360*	1.0mV	1µA	40mA	50MHz	800V/µs
LT1363*	1.5mV	2µA	70mA	75MHz	1000V/µs
LT1457	800µV	75pA	10mA	1.7MHz	4V/µs

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chip—the BD-1?" Roy spun around: "How did you know that?" I tried to explain that it was just an April Fool joke. That made Roy even madder. Then we realized that the silly customer didn't realize it was an April Fool joke, as he could not find where it was announced in the magazine. That really got him mad! Roy was mad at Bob Dobkin, and, it seemed, at the rest of the WORLD for several YEARS.

Ham radio guys are always inventing and building equipment, so they're prime targets for pranksters. In 1966, Tom Kneitel published plans in *S9* magazine for a small, low-cost antenna made of two 100-Ω resistors.

He claimed that "it has the lowest possible VSWR across the entire band with a perfect match to any rig; exhibits an omni-directional null radiation pattern; eliminates adjacent channel overload from strong local signals; may be used either horizontally or vertically; completely ends TVI problems; is impervious to auto ignition noise; and has maximum efficiency at any height. Rust-, corrosion-, and lightning-proof, it can be carried around in your pocket for walkie-talkie use."

Of course, many Hams built it and complained that they could not get this antenna to transmit or receive *anything*. Exactly.... a dummy load. Other famous April Fool stories are about tall antennas that can't be seen due to use of stealth paint, etc.

When Nikolai Tesla invented the ac induction motor in 1877,[5] which ran with no brushes and no commutator, it was greeted with severe skepticism—must be a hoax. I'm sure if I had been there, I would have been incredulous, too. However, some of the later claims of Tesla border on the bizarre, and may fall over into hoaxery. Claims that electricity can be transmitted around the world with no losses, megavolt sparks under complete control, and an oscillator with an output of 10,000,000 horsepower were pretty wild, impossible to duplicate, and pretty hard to prove or disprove, theoretically or otherwise.

Heck, that reminds me of the April Fool circuit that was alleged to cause the end of the world if turned on. Some guy wrote that he built it and pushed the button, but complained that the world did *not* end when he pushed the button. Tesla's ghost??

Because I'm not knowledgeable about Software, I will not have much to say here, except to quote from a News Release—*Vogon News*[6]: "In an announcement that has stunned the computer industry, Ken Thompson, Dennis Ritchie, and Brian Kernighan admitted that the UNIX operating system and C programming language created by them is an elaborate April Fools prank kept alive for over 20 years.... 'As a lark, we decided to do parodies of the Multics environment and Pascal... we stopped when we got a clean compile on the following syntax:

```
for(;P(“\n”),R-;P(“|”))for(e=C;e-;P(“_”
+(*u++/8)%2))P(“|    ”+(*u/4)%2);
```

"To think that modern programmers would try to use a language that allowed such a statement was beyond comprehension! We actually thought of selling this to the Soviets, to set their computer science progress back 20 or more years. Imagine our surprise when AT&T and other U.S. corporations actually began to use Unix and C!.....' " Beyond that, RAP has no comment. (Complete details available from RAP with SASE.)

In another case of subterfuge, a friend gave me a copy of a Special Announcement—"After a long period of research and development, Mohawk Engineering announces a revolutionary new switch and charging system... which allows a battery system of any type to supply power to a load or device while automatically and simultaneously allowing the battery to recharge itself." Complete blueprints can be obtained for just $100 from a post office box in Springfield, Mass.

Back in 1958, some engineers were quite unhappy about the quality of papers being published at conferences, so they wrote up a marvelous piece of puffery about their new "Linistor." This paper was accepted at WESCON. Then they revealed that their new invention was an alternate way to describe the *resistor*. Their prank had the desired effect when technical conferences began screening the papers more closely.

Recently, a Reviewer was evaluating a "Scantrack 18 Golfball Finder".[7] After diligent and fruitless efforts to find any "output" from this little $89.95 gem, which uses "new microchip technology" to detect the "molecular wavelengths emitted by golf balls," he got mad and X-rayed it, and found it completely empty. No circuitry at all. Wonderful hoax.

What was the year—1978?—when Signetics brought out the WOM—the Write-Only Memory? Not just any simple April Fool joke, this marvelous invention was professionally presented in full color in a four-page foldout section of electronics magazines. Even us Analog guys got a good giggle out of that one! I've occasionally wondered what $ was paid for the publication of that fine joke—and by whom!!

One does still see, in cheap magazines and on odd radio stations, advertisements for the little box that "turns your house wiring into a giant TV antenna." I asked my friends who are knowledgeable about TV and ham radio. One said it was just stupid, because it did all of the wrong things with the signals. Another guy said its theory was dubious, but actually he had seen it work better than a rabbit-ears antenna. *Consumer Reports* says this kind of antenna usually does more harm than good[8]—a bad investment for $1.99 in 1973, and a bad investment for $19.95 in 1994.

At least one guy thinks that ISO 9000 is a first-class hoax. I will admit that we may be forced to conform to the minimum requirements of these regulations drafted by a bunch of European bureaucrats, in order to do business with Europe. However, I agree with George Lohrer of Programmed Test Sources Inc.[9] that some of the zeal we see for super-compliance and "we can meet ISO 9000 better than you can" is pretty disgusting. Copies of his letter available from RAP per SASE.

One of my readers spotted a case where a hobby magazine ran a build-it-yourself article. A special 24-pin IC, available from the author for just $30, was used to make an interface be-

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tween a Macintosh computer and an ordinary video display. However, the actual circuitry inside this 24-pin IC was just a 7404 inverter IC, encapsulated with a funny pin-out. Ahem.

Obviously, I don't know half of the good electronic hoax stories in the world, but, hey, we have run out of room, so we will just print what we got. If you know a better one, we may run it next year.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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Santa Clara, CA 95052-8090

1. *Encyclopedia of Hoaxes*, Gordon Stein, Gale Research, Detroit, 1993. ISBN # 0-8103-8414-0. About $49.95; phone: 800-877-GALE; fax: 313-961-6083.
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3. "Energy machine floats in perpetual limbo among agencies, court," *Electronic Design*, July 24, 1986, p. 155.
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7. "Scantrak 18 Golfball Finder," $89.95 from Lil' Orbits Inc., Minneapolis, MN. Reviewed in *Popular Electronics*, Jan. 1994.
8. *Consumer Reports*, Jan. 1989, p. 5.
9. "ISO 9000: Barking up the Wrong Tree?," Letter to the Editor by George H. Lohrer, President, Programmed Test Sources, P.O. Box 517, Littleton, MA 01460; published in *RF Design*, Oct. 1993, p. 14.

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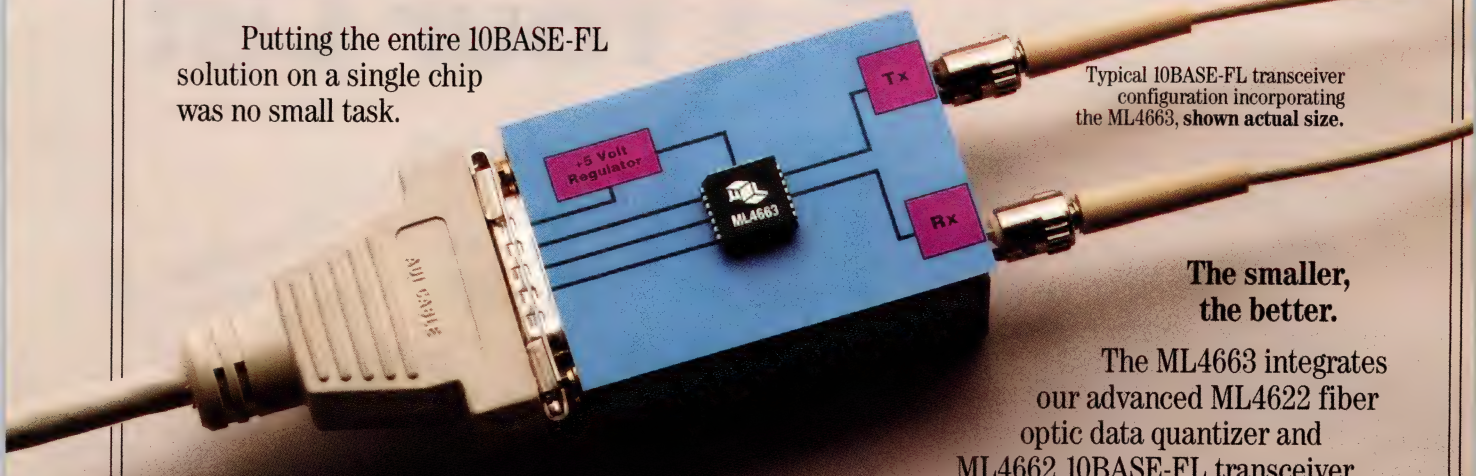

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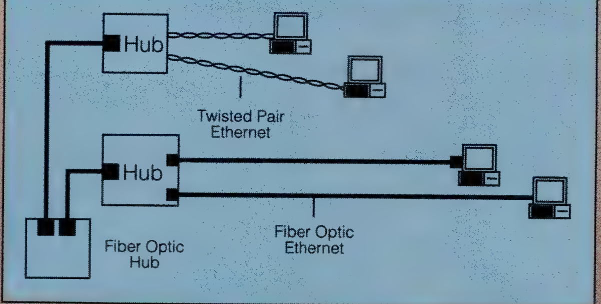

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UPDATE

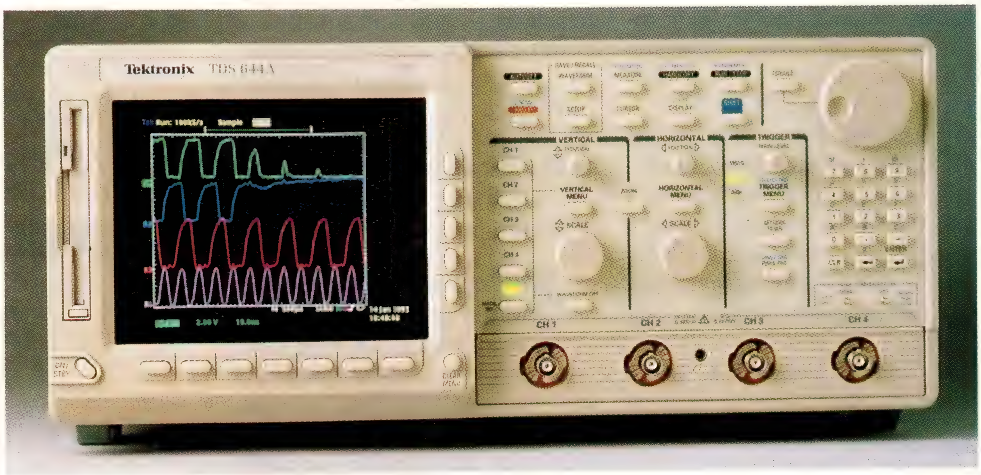
TEST & MEASUREMENT

A SPECIAL EDITORIAL FEATURE

DSOs Take A Technological Leap

With higher performance and lower prices, digital scopes give users more measurement flexibility.

BY JOHN NOVELLINO



Digital-storage-oscilloscope technology is the fastest moving area in test and measurement today. Users are reaping the benefits of advances in all categories of DSO technology: acquisition systems, the core processing systems, automated measurement capability, and displays.

Now users can choose from among instruments that are more general purpose than ever (being able to make many measurements that once required multiple systems), or from instruments that can be nearly application-specific for complex measurement tasks. Better yet, the prices for these technologically advanced instruments are coming down. This type of trend is very similar to one well known to personal-computer users: Customers can expect to get greater performance for the same price or the same performance for less money.

Typically, the first concern engineers have when they discuss digital oscilloscopes is the acquisition system. They want to know whether a scope that uses a sampling technique can accurately capture the signals they need to see. In a DSO, that accuracy takes two forms—amplitude (vertical) accuracy and timing (horizontal) accuracy. A major component of the former is the vertical resolution, which has pretty much standardized at 8 bits. However, 10- and 12-bit instruments are available and averaging techniques can improve effective resolution. Overall vertical accuracies within 1% are possible.

The timing accuracy is more problematic. Although such factors as clock precision and jitter are important, the specification most users concentrate on is sampling rate. DSO manufacturers have made a strong effort to ease those concerns, with some major breakthroughs in sample-rate performance. Sample rates as high as 500 Msamples/s are available at more reasonable prices than even a year or two ago, and 1-Gsample/s and faster scopes are also more prevalent *(see the chart, p. 107)*.

The greater availability of higher sampling rates will help users by reducing the number of times when they question the accuracy of the displayed waveform and how it was acquired. "The user is no longer having to think about the technology, like when am I operating in real-time mode and when am I operating in equivalent-sampling mode," says Chris Martinez, marketing manager for oscilloscopes at Tektronix, Beaverton, Ore. "As the sample rates are starting to match the analog bandwidth of the instrument, you no longer have to think about it. It always gives you more of what you want to see on the display."

Acquisition memory is also an area that has seen recent advances. In newer DSOs, memories of 2 or 4 kpoints per channel are the rule, replacing the once common 1 kpoint per channel. More scopes now are available with 10-kpoint and longer memories as either standard or optional, and some instruments have megapoint-level storage capacities. Deep storage is important at today's faster sampling rates, because it eliminates the need to choose between a very short acquisition time or slowing down the sampling rate.

One particularly useful advance is the ability to interleave individual channel memories. A number of DSOs interleave analog-to-digital converters so that, for example, a two-channel, 50-Msample/s instrument can digitize at 100 Msamples/s on one channel. Interleaving memories have been available on a few very expensive DSOs, but now are being incorporated in DSOs priced under $10,000. This includes the LeCroy 9350 series, which can interleave both converters and memories.

Although in principle it's not difficult to interleave DSO memories, in practice it's not a trivial task. "It's not easy to take gigasample per second type signals coming in every nanosecond and switch between one memory bank and another," says Michael Lauterbach, director of product management at LeCroy, Chestnut Ridge, N.Y. "And people say that memory is cheap, but nanosecond memory is not cheap."

What these advances constitute is a trend toward faster, deeper, and cheaper (sampling rate, memory, and price). Users can expect more of the same from most manufacturers, but not from Fluke Corp., according to Charles Holtom, who does product marketing for the Everett, Wash. company's oscilloscopes. Although DSO banner specifications like sampling rate and memory are increasing rapidly, Holtom says that's not enough.

"The user is being told that an oscilloscope sampling at 500 Msamples/s can replace an analog scope," he says. "But we don't say that. We don't believe that is true." Fluke feels that no digital scope on the market can give as faithful a representation of a repetitive signal as an analog scope can, he says. As a result, the company will continue to build its line of CombiScopes, which include full analog as well as digital capability. Holtom believes it will be three to five years before digital scopes will come close to eliminating the need for analog instruments.

People want digital scopes for three reasons, says Holtom—to catch single-shot events; to capture high-speed, low-repetition events; and to be able to send the acquired signals to a computer or hard-copy device. "That is the real value of a DSO, the information can be processed," he says. That being the case, scope designers should concentrate on making DSOs as easy as possible to use, with minimum reliance on multilevel menus, and with as much automated measuring ability as possible. That's the direction Fluke intends to take, says Holtom.

All of this acquisition power would be wasted if the instruments' core processing systems weren't keeping pace. A key complaint users voiced about some older designs was that they didn't have the real-time feel of analog oscilloscopes. The result is increased use of multiprocessor control systems, with ever more powerful processors. Separate processors for acquisition, display, and signal analysis eliminate time-sharing among these functions and boost update rates.

Together with direct-access knob controls, this processing power helps provide the "live" feel users desire. "If you're troubleshooting and you're moving the probe around trying to find out what's wrong with your circuit, you don't want to stop and think, 'Is this an alias I'm seeing or is it the real signal?' " says Jerry Murphy, product marketing engineer with Hewlett-Packard's Personal Measurement Operation. "So we really work hard at giving the customer that real-time feel of what's going on at the probe tip."

Fortunately, the price of processing power continues to drop, making it easier for DSO designers to add more digital-signal processing to their instruments. Some users want a choice between linear or straight-line interpolation and (sine x)/x interpolation, says Tektronix's Martinez. He states that including a separate DSP function in scopes gives users this choice without slowing down performance.

DSOs now do much of the number crunching that once was done externally.

The more readily available computing power also has boosted a DSO's ability to supply users with multiple, calculated measurements, not just raw data. Many users still employ scopes for basic troubleshooting tasks, where looking at signals at various locations and settings is the prime consideration. But a growing number are using DSOs to verify and characterize circuit performance.

For these more complex setups, DSO manufacturers are designing into their instruments much of the number crunching that once was done externally. "Test equipment vendors are trying more and more to supply customers with answers at a higher conceptual level," according to Bob Berry, product manager for oscilloscopes at HP's Colorado Springs Div. "If you look at the number of people who are hooking our products and other similar products to PCs and extracting information out of the basic-instrument environment and into a computing environment, that'll give you an idea of how specialized some of our customers' applications are getting."

Scope designers must pull these diverse functions together to get the maximum benefit from them. "It's important that a scope have a very high throughput and be very responsive to user commands," says Berry. "Being able to tightly integrate the acquisition system, core CPU, and display systems together gives customers that interactive, high-throughput environment."

One problem on the rise is probing. The electrical characteristics of probes are obviously a factor if users are to take advantage of wide-bandwidth DSOs now available. But a probe's mechanical design is also important as component geometries get smaller and board densities increase.

The problem is compounded by the higher operating speeds desired by designers. As they find out how difficult it is to move high-speed signals across pc boards and through backplanes, designers opt for higher-density components. Consequently, designers of high-performance scopes are constantly striving to come up with better ways to nonintrusively probe the circuits under test.

The question of the bandwidth itself can come as a shock to some scope users. Designers working with processors running at 25 or 33 MHz and above generally must probe signal characteristics as well as functionality, because timing considerations become critical at high speeds.

A good rule of thumb is that the scope's bandwidth should be at least 10 times the signal's fundamental frequency to accurately represent such signals. That puts a suitable instrument in the 300-MHz range.

The signal's rise time also is a factor, however. To faithfully capture a 1-ns rise time, Tektronix's Martinez explains, designers may need a 500-MHz scope. "We believe there's a whole new set of people who have crossed this threshold into high speeds and their textbook digital design classes in college perhaps didn't dwell on this too much," he says. "We like to tell them, 'This is all analog, folks, and your digital thought processes need to change.' "

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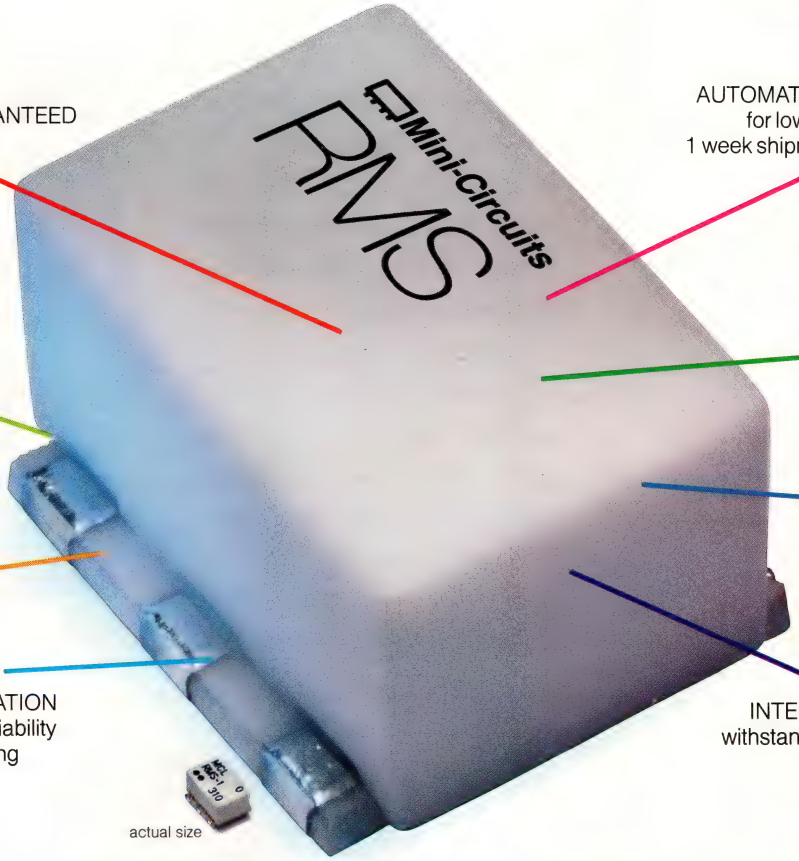

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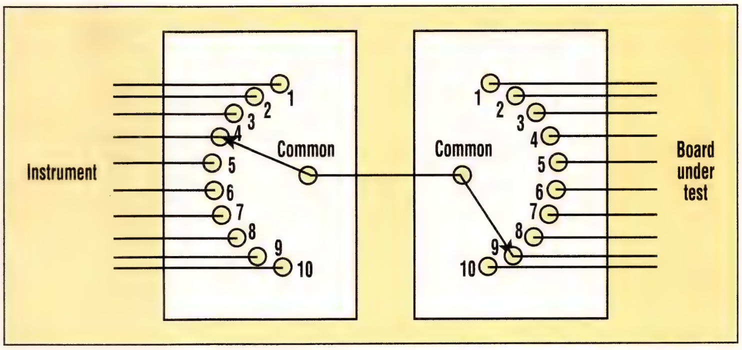
Switch Matrix Simplifies Scope Setups

An IEEE-488-controlled matrix makes possible automated board testing with a bed-of-nails fixture.

BY ROBERT BOMBARA

Teradyne Inc., 179 Lincoln St., Boston, MA 02111; (617) 422-3794.

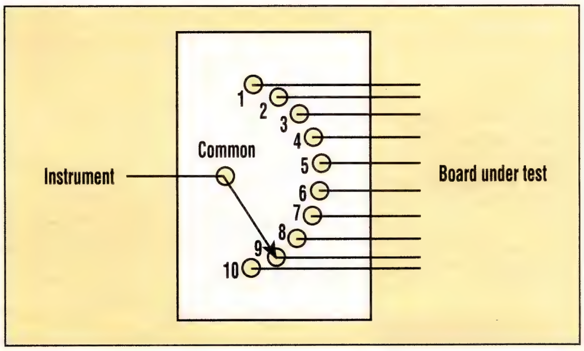
Modern digital oscilloscopes are remarkable instruments that can be used for edge characterization, time-domain reflectometry (TDR), and pulse parameter measurements well into the picosecond range. The bad news, however, is that getting signals from a device under test to the scope isn't a trivial task. Routing these signals under software control eliminates manual setups, reduces test times, increases the reliability and repeatability of the measurements, and creates a fully automated test process. The IEEE-488-controlled RF switching matrix described in this article offers designers this capability for board testing.



2. A common-highway matrix multiplexes more than one instrument to more that one test point, but only one instrument at a time can be used.

Also discussed are the design considerations, which include the mechanical interface between the matrix and the fixture, as well as some probing techniques. Rounding things out are some ideas for a more advanced matrix. Such a matrix could be used to multiplex more than one instrument and would form the nucleus of a completely hands-off performance test setup.

A tour through a typical test floor may well uncover two very different test processes. On one side, technicians are surrounded by GPIB-controlled rack-and-stack equipment connected to the board under test (BUT) by a tangle of cables and scope probes. This equipment augments a functional board test system and is generally used after thorough testing with in-circuit and functional ATE.



1. The simplest type of switching matrix, called a switch-tree matrix, uses a single-pole, multiple-throw switch to connect several test points to one instrument, or vice versa.

Typically, such equipment accesses the BUT through edge-connector fixturing, so test programs require setup instructions that direct the operator to probe certain points and make various connections. These manual setups are undesirable, because they increase test time, are prone to operator error, and lead to signal degradation as connectors wear out.

The other side of the test floor holds in-circuit or combinational testers. On top of these machines sit vacuum bed-of-nails test fixtures with spring-loaded probes under each node of the BUT. Twisted-pair wiring connects these probes to tester channels. Under software control, the tester channels multiplex the tester's resources. Such a setup makes the connection to the BUT transparent to the operator. As a result, these test programs usually need no setup messages and require limited operator involvement.

The switching matrix described in this article uses some RF switching circuitry to multiplex four scope channels and a trigger to 45 spring probes in a vacuum bed-of-nails fixture. The RF switching matrix marries the speed and reliability of hands-off testing made possible by the vacuum bed-of-nails test fixture to the high-performance measurements of today's rack-and-stack equipment.

Using a switching matrix and vacuum bed-of-nails fixturing increases both test throughput and yield. The technique eliminates the need for scope probes, clip leads, and DIP clips. This is advantageous because clipping a scope probe onto a lead of a through-hole IC without shorting the adjacent leads requires the hands of a surgeon. When the probe falls off halfway through a test, the situation can get ugly. If the wrong point is probed, a good board could be falsely indicted, or a bad board could ship to the field.

In some test situations, vacuum bed-of-nails fixturing is more than just preferable, it's absolutely necessary. Some devices—including relays, oscillators, gate arrays, and connectors—have leads directly under the device package. This type of lead can't be accessed with any type of clip-on probe, but can be easily accessed with a spring probe contacting the underside of the board. Fine-pitch surface-mount ICs also are very difficult to access with anything but a spring probe.

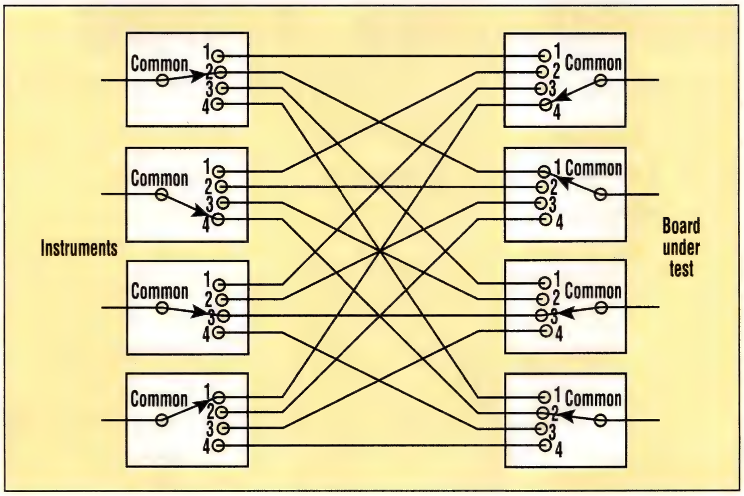
The example matrix design is a type of matrix commonly called a "switch tree." The simplest switch-tree matrix is implemented with one single-pole, double-throw (SPDT) switch to create a 1-by-2 switch tree. But a multiple-throw device is typically used, so that the operator can multiplex several test points to one instrument or several instruments to one test point *(Fig. 1)*.

The switch tree's drawback is that it can't multiplex more than one instrument to more than one test point. This can be solved, though, by combining two similar switch trees into a "common-highway" matrix *(Fig. 2)*. By using such an arrangement, multiple instruments can be multiplexed, but only one instrument at a time can be used.

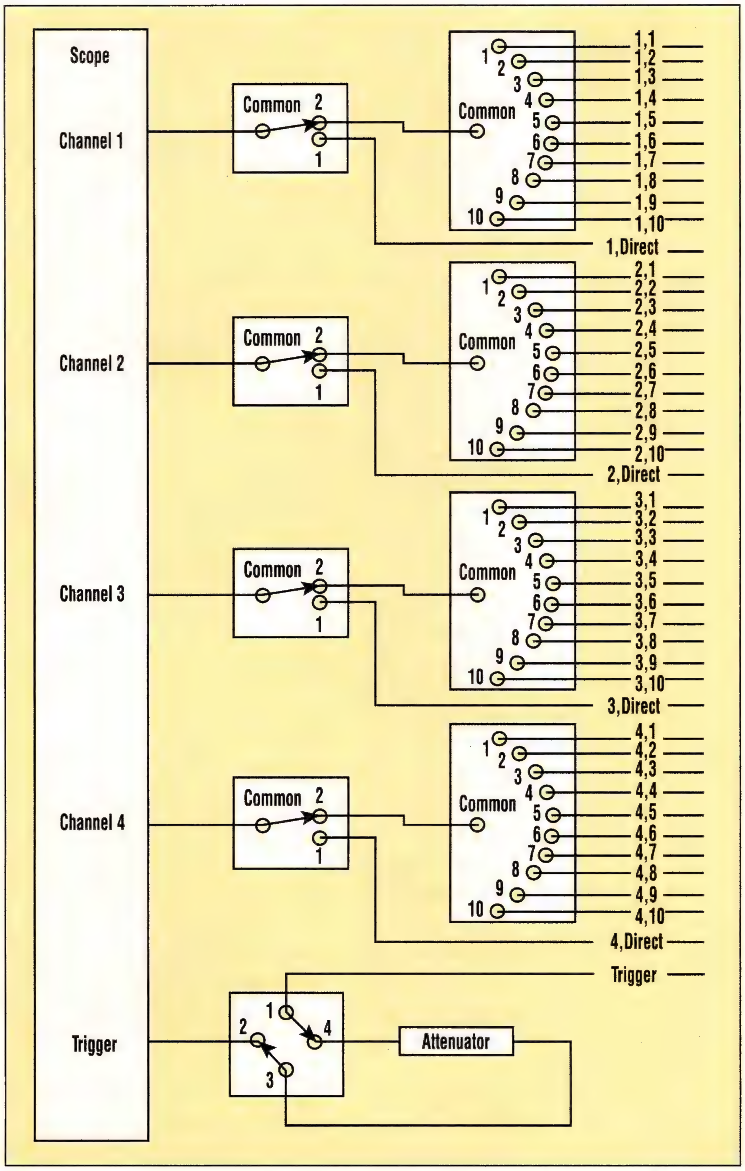
Because most tests require both a source and a measurement instrument to be active simultaneously, the common-highway matrix has limited usefulness. A full-crosspoint matrix resolves this problem, allowing all inputs and outputs to be used at the same time *(Fig. 3)*. The cost of a full-crosspoint matrix, however, becomes prohibitive because one switch is needed for each input and output.

The example matrix supplies a 1:11 multiplexing ratio for each scope channel, and a switchable attenuator for the trigger line *(Fig. 4)*. Tests performed with a digital scope have improved dramatically using this switch-tree configuration. SPDT relays were placed between the scope inputs and 10-throw multiplexing relays to create an ultra-high-bandwidth path to each input. These SPDT relays also allow for some interesting setup configurations, which will be discussed later.

Because the 10-throw switches are normally open devices, the scope inputs are effectively isolated from the BUT upon test program initialization. In prac-



3. A full-crosspoint matrix, like this 4-by-4 example, allows users to connect any of several instruments to any output simultaneously, but at a significantly higher level of complexity and cost.



4. Based on a switch-tree configuration, this matrix supplies a 1:11 multiplexing ratio for each of four digital scope channels and includes a switchable attenuator for the trigger line.

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tice, power is applied to the BUT before any connections are made to the scope. This sequence ensures that any static charge present on the BUT dissipates before it can damage the unprotected gallium-arsenide scope inputs.

Prior to installing the matrix, scope inputs had been damaged several times, and many hours were wasted searching for substitute idle scopes to be employed in test programs. During the matrix's 18-month lifetime, no scope input has been damaged by static discharge.

The relays were selected primarily for their high bandwidth. The 10-throw switches have an insertion loss of only 0.8 dB to 18 GHz. The SPDT switches have a 0.6-dB insertion loss to 22 GHz, and the transfer switches' loss is 0.5 dB to 18 GHz. The relays are housed in a 19-in. rack-mount enclosure.

In addition to controlling an RF switch, each relay coil controls an indicator switch. These indicator switches drive red LEDs mounted on the front panel to visually indicate the status of each relay. Individual LEDs were chosen instead of seven-segment displays so that multiple relay closures in a 10-throw package could be displayed more easily. Using the relay coils to control indicator switches guarantees that the LEDs won't light unless there's an actual switch closure.

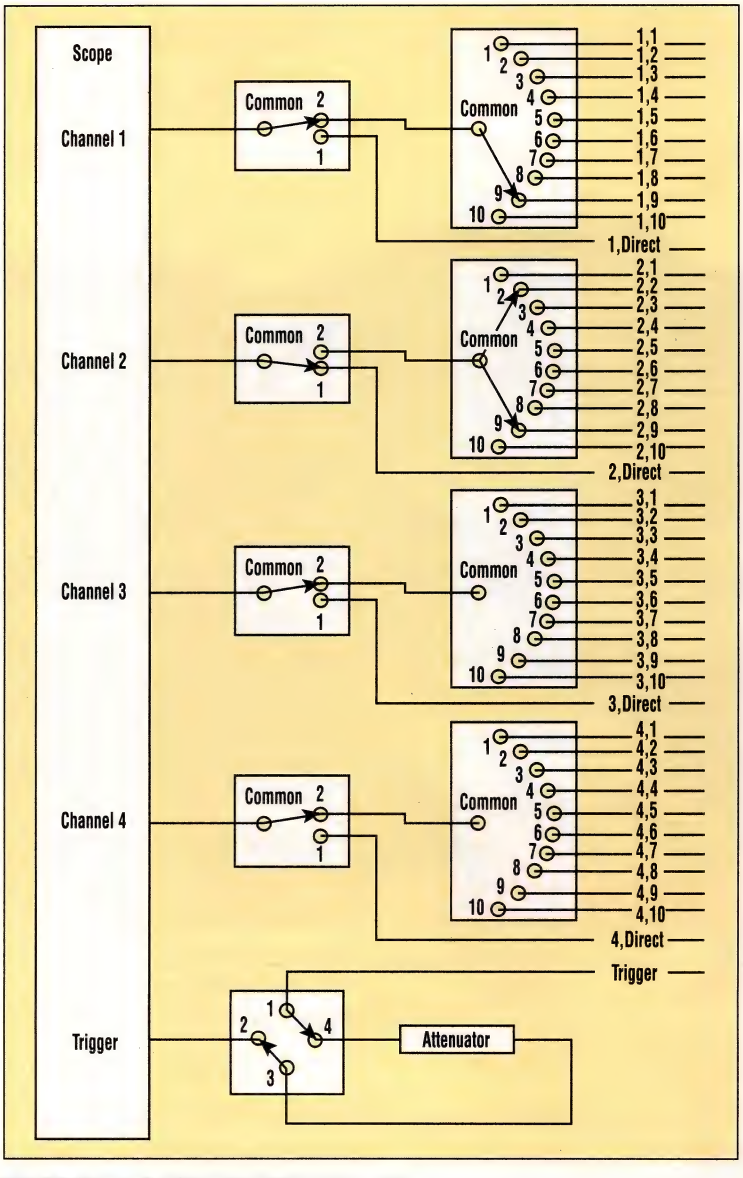
The enclosure also houses a 28-V power supply for the relays, a cooling fan, and the logic that links the relays and the GPIB relay controller. The enclosure measures about 18 in. wide by 9 in. high. by 17 in. deep. Such width and height are needed to accommodate both the relays and the LEDs on the front panel.

Other matrices that had relays mounted on the rear panel were examined. This configuration, however, requires much longer cables to reach the fixture. The resulting increase in insertion loss and capacitance makes this arrangement less desirable. The rather deep enclosure is needed for the large linear power supply selected. Using an equally powerful switch-mode supply could easily cut this dimension in half.

An off-the-shelf external GPIB relay controller controls the matrix. The controller supplies 56 bidirectional control lines—45 control the state of the relays while the remaining 11 monitor the state of the relays. These 11 monitor lines also tie into the relay indicator circuits so that the lines only indicate actual mechanical switch closures. Designing a controller in-house was considered but eventually got dismissed because of the time penalty involved.

Use of an internal OEM controller board also was rejected because integrating a controller board into the matrix enclosure would require a major mechanical redesign if and when a VXI version of the matrix is developed. As designed, a new wiring harness would be the only hardware change needed to switch from a GPIB controller to a VXI controller card. At least one vendor already sells a B-size VXI controller card well suited for this application.

The relay controller is itself controlled with a software driv-



5. In this variation of the 1:11 switching matrix, the channel 1 and channel 2 10-throw relays were rewired to multiplex 16 test points into one scope channel.

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er developed in-house. However, the actual GPIB string commands for the controller are so simple that the driver appears to be more a luxury than a necessity. For example, the command "close 100; < CR > " is all that's required to connect channel 1 of the scope to position 1,1.

The connections between the RF relays and the fixture connector block are made with 23-in. SMA cables rated for a 0.96-dB loss up to 22 GHz. Although this isn't spectacular performance, the cable's small outer diameter makes it well suited for use in tight quarters. To reduce crosstalk, the cables were left loose instead of being bundled together.

The fixture connector block is a cam-actuated floating rectangular plate that carries 64 blind-mate connectors arranged in six rows. The 64 connectors, which provide the interface for the matrix and the other instrumentation in the rack, can tolerate a maximum of 0.020-in. radial misalignment. In addition, the connector plate supplies another 0.130 in. of radial float, which allows the system to accommodate fixture-to-fixture dimensional variation.

Each connector requires an insertion force of 3.4 lbs. to fully actuate. The force generated by 64 of these connectors on the back of a vacuum bed-of-nails test fixture would create a bowing, which would thus prevent complete connector insertion. Consequently, the fixtures are braced where needed to minimize bowing.

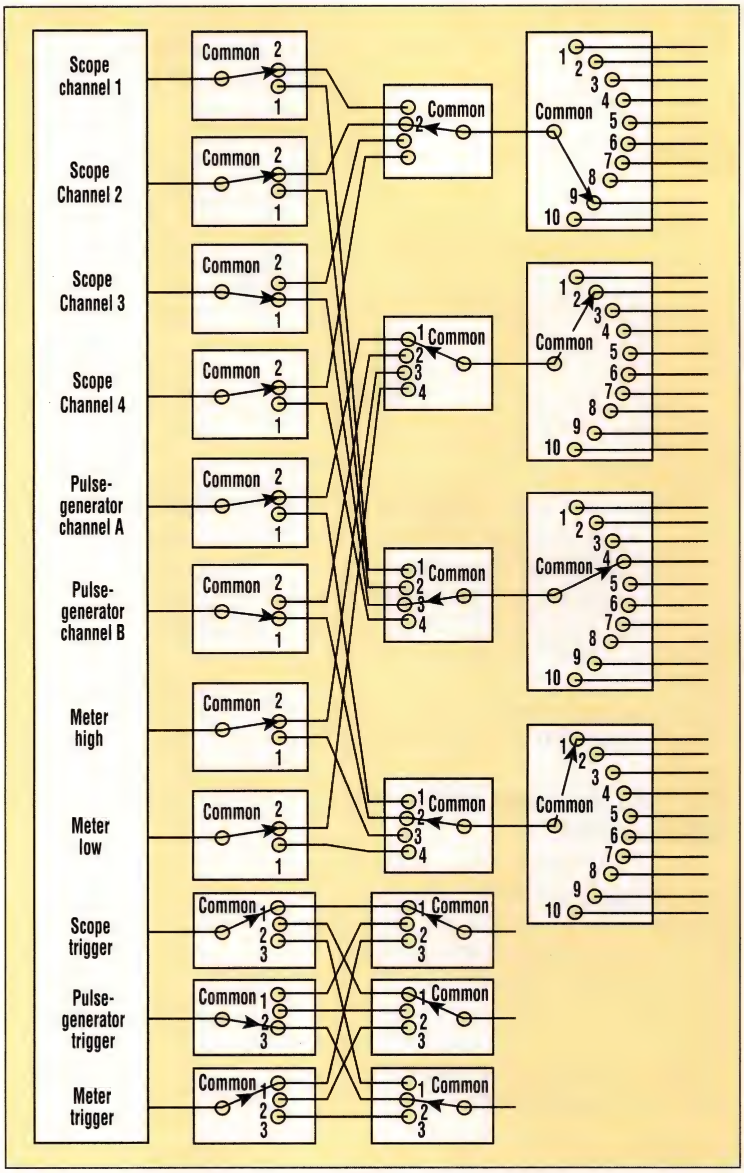
The vacuum bed-of-nails fixture offers excellent accessibility to all nodes of the BUT. The blind-mate connectors are linked to the spring probes by RG-316 coaxial cables. This cable's small diameter allows for small bend radii, making it an excellent choice for the crowded area under a test fixture.

Connecting the coax directly to the tail of a spring probe is undesirable because the reflections caused by the resulting stub would severely degrade the signal. Also, when probing an ECL node, the spring probe would appear as a 50-Ω pull-up to ground. Both of these problems can be solved by adding a 450-Ω non-inductive resistor in series with the spring probe tail and the center conductor of the coax. Combining a 450-Ω resistor with a 50-Ω scope input forms a 10:1 divider circuit, which reduces reflections and output loading.

Over the years, this setup has proven to be a much more cost-effective solution to probing as opposed to using an active probe at each node. In a few cases where the 10:1 attenuation ratio was insufficient, 950-Ω resistors were used to create a 20:1 attenuation. This further reduced circuit loading and reflections, but, of course, yielded a smaller signal at the scope input. Employing small trim capacitors results in still better edges, but their use is beyond the scope of this article.

As previously mentioned, using an SPDT and a 10-throw switch to create an 11:1 multiplex ratio makes it possible to exploit some interesting configurations. In one application, 16 test points were multiplexed into one scope channel to take advantage of its TDR function.

6. This matrix mixes several techniques so that more than one instrument can be connected and used simultaneously. It takes advantage of the fact that not all instruments need an expensive high-bandwidth path, that not all instruments are needed on all test points, and that trigger inputs don't need access to all test points.



The test points were divided into two groups of 8. The first group was wired to positions 1,1 through 1,8 of the matrix and was tested normally. The second group was wired to positions 2,1 through 2,8 with a jumper inside the fixture connecting positions 1,9 and 2,9 *(Fig. 5)*.

By energizing positions 1,9 and 2,9 and switching SPDT 2 to 2,Direct, the inputs from positions 2,1 through 2,8 were effectively switched into channel 1 of the scope. Note that multiple positions in each 10-throw switch package may be simultaneously connected to the "com" position. Also note the stub created between SPDT 2 and 10-throw 2. The stub was noticeable as a "bump" on the scope's TDR display, but wasn't large enough to hinder the measurement.

A switching matrix and vacuum bed-of-nails fixture increase test throughput and yield.

The RF switching matrix significantly improved tests using the digitizing oscilloscope. A state-of-the-art functional test setup, however, utilizes many more instruments than just a scope. Consequently, a matrix that can multiplex several instruments would be useful. As noted, a full-crosspoint matrix offers complete flexibility to connect any instrument to any input, but this solution is costly.

Fortunately, not all inputs and outputs are needed at the same time. With some thought, it quickly becomes apparent which instrument functions, and, therefore, which matrix lines must be available at any given time. In addition, the instruments' trigger inputs most likely don't need access to all of the test points. For example, a particular test may require oscilloscope measurements on 10 different outputs, all derived from one master clock signal. In this case, the scope's trigger input would simply be connected to the clock source.

Finally, not all instruments will need a high-bandwidth path. A meter used to make dc and resistance measurements could use low-bandwidth and, hence, less expensive relays. As a result, a practical matrix may contain a mixture of all the aforementioned matrix types. One such example would be a matrix that connects an oscilloscope, pulse generator, and meter to 43 test points *(Fig. 6)*. It would be an excellent choice for a state-of-the-art test setup.

Robert Bombara, test engineer for Teradyne, received his BSEE from Worcester Polytechnic Institute, Worcester, Mass.

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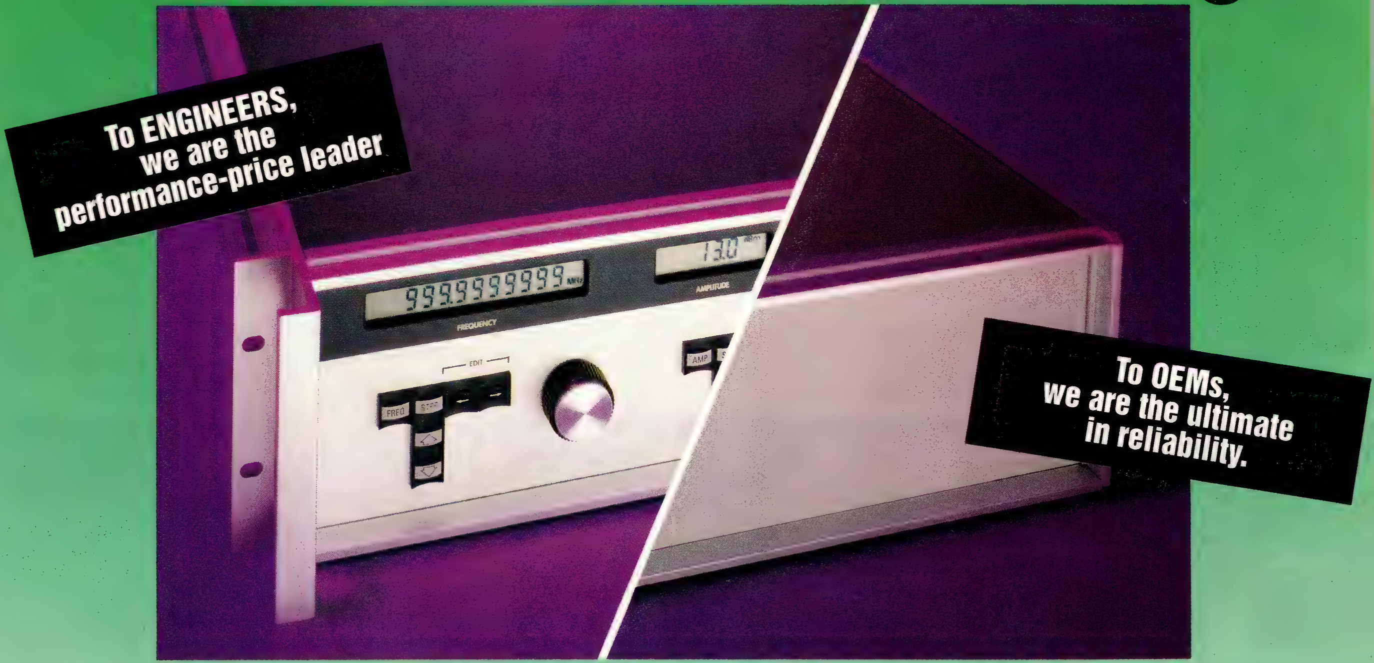
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13.0 dBm
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FREQ
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PTS synthesizers were designed from the outset to deliver the best reliability in the business. We adhere to conservative derating practices, keep power consumption and internal heat buildup to an absolute minimum and subject finished systems to rigorous temperature cycling and electrical testing. The result: a field-proven 25,000 hr MTBF. Since 1985 we've offered a full 2 year warranty and a flat-rate repair fee of just $350 for years 3 through 10.

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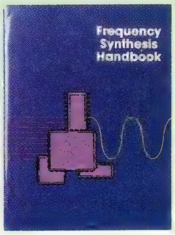

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PTS

PROGRAMMED TEST SOURCES, INC.
9 Beaver Brook Road, Littleton, MA 01460
Tel: 508 486-3008 Fax: 508 486-4495

READER SERVICE 104

▼ FAST DIGITAL SCOPE GETS 33-MHZ PROCESSOR

The Model 9360 digital oscilloscope has been upgraded with a 33-MHz 68030 processor board that replaces the original 16-MHz 68020 board. The 9360 captures signals at a 5-Gsample/s sampling rate in single-shot mode. Included on the two-channel scope are several features aimed at laser measurements. With the new board, these functions are performed two to three times faster. The faster board has been added as a standard feature at the scope's $12,490 price. Customers who already ordered the scope will receive the board at no charge.

LeCroy Corp.
700 Chestnut Ridge Rd.
Chestnut Ridge, NY 10977-6499
(914) 425-2000
▶CIRCLE 750

▼ BENCHTOP DMM FEATURES ±0.03% DC ACCURACY

The Model BDM40 is a 4-1/2-digit, true-RMS benchtop digital multimeter with a basic dc accuracy of ±0.03% of reading. Five ac and dc voltage ranges run to 1200 V, and six ac and dc current ranges cover to 2 A. The 2-A jack is fully fused. The meter also measures resistance to 20 MΩ in six ranges and includes a diode test function. The true-RMS function is push-button selectable for ac or ac + dc coupling to ensure accurate readings regardless of waveforms. Results are displayed on an LED display in 0.5-in. red digits. The BDM40 is available from stock for $429.

Wavetek Corp.
9045 Balboa Ave.
San Diego, CA 92123
(619) 279-2955, ext. 332
▶CIRCLE 751

▼ COUPLERS AID POWER MEASUREMENTS TO 1 GHZ

Two dual (bidirectional) couplers let users monitor both forward and reflected power between any transmitter and load, including RF power amplifiers and antennas, through an 80-MHz-to-1-GHz bandwidth. The DC6180 handles 600 W of continuous power (1000 W peak), and the DC6280 carries up to 1500 W of continuous power. Both units have a typical directivity of 25 dB and insertion loss of 0.15 dB maximum. The coupling factor is 60±1 dB for the DC6180 and 63±1 dB for the DC6280. The DC6180 costs $900 and the DC6280 is $1100.

Amplifier Research
160 School House Rd.
Souderton, PA 18964-9990
(800) 933-8181 or (215) 723-8181
▶CIRCLE 752

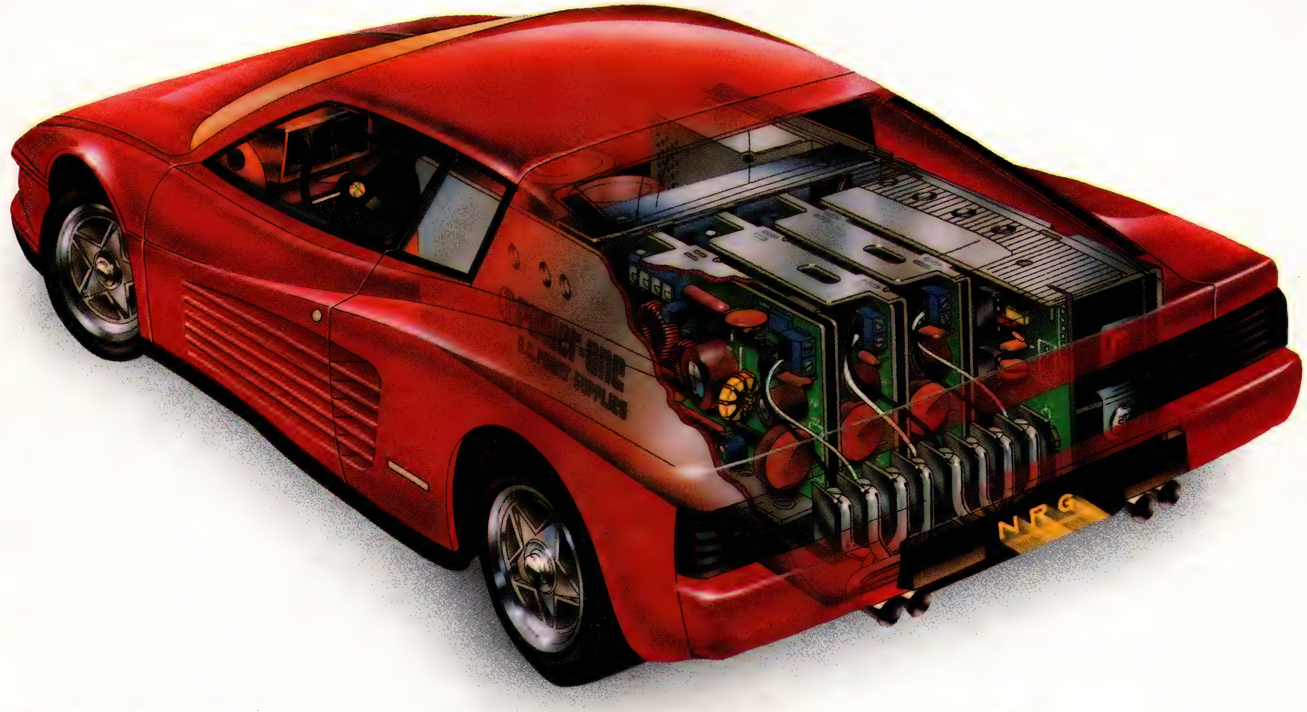
DIGITAL STORAGE OSCILLOSCOPES

Manufacturer	Model/price	Sample rate (Msamples/s)/ Vertical resolution (bits)	Repetitive/ single-shot bandwidth (MHz)[1]	Channels/ Record length (samples)	Remarks
B&K Precision 6470 Courtland St. Chicago, IL 60635 (312) 889-1448	2522A/$1099	20/8	20/4	2/2k per ch.	Linear interpolation, analog mode; plotter outputs.
Fluke Corp. P.O. Box 9090 Everett, WA 98206-9090 (800) 443-5853	PM3335/$1950	20/8	N.A./2	2/8k	Analog mode; automated measurements; IEEE-488, RS-232 opt.
	PM3350A/ $3250	100/8	N.A./10	2/4k	Analog mode; automated measurements; IEEE-488, RS-232 opt.
	PM3365A/ $3750	100/8	60/10	2/4k	Analog mode; automated measurements; IEEE-488, RS-232 opt.
	PM3355/$4650	250/8	N.A./25	2/4	Analog mode; automated measurements; IEEE-488, RS-232 opt.
	PM3375/$4750	250/8	100/25	2/4k	Analog mode; automated measurements; IEEE-488, RS-232 opt.
	PM3382/$4990	200/8	100/20	2+2/8k	Full analog mode; automated measurements; RS-232 standard; IEEE-488, additional memory, math opt.
	PM3384/$5490	200/8	100/20	4/8k	Full analog mode; automated measurements; RS-232 standard; IEEE-488, additional memory, math opt.
	PM3392/$5990	200/8	200/20	2+2/8k	Full analog mode; automated measurements; RS-232 standard; IEEE-488, additional memory, math opt.
	PM3394/$6490	200/8	200/20	4/8k	Full analog mode; automated measurements; RS-232 standard; IEEE-488, additional memory, math opt.
	PM3384E/ $7160	200/8	100/20	4/32k	Full analog mode; automatic timebase mode; timebase in time/div. or deg./div. for engine monitoring; frequency or rpm readout.
Goldstar Precision Co. Ltd. 13013 E. 166th St. Cerritos, CA 90701 (310) 404-0101	OS-3020/ $1295	20/8	20/5	2/2k	CRT and cursor readout; RS-232 output.
	OS-3040/ $1795	20/8	40/5	2/2k	CRT and cursor readout; RS-232 output.
	OS-3060/ $2195	20/8	60/5	2/2k	Alternate magnitude and go/no-go CRT and cursor readout; RS-232 output.
Gould Instrument Systems Inc. 8333 Rockside Rd. Valley View, OH 44125 (216) 328-7000	400/$2290	100/8	20/20	2/512 per ch.	Serial interface; battery, IEEE-488.2 opt.
	420/$2390	100/8	20/20	2/512 per ch.	Same as Model 400 plus automatic measurements, persistance display; 4-color plotter opt.

DIGITAL STORAGE OSCILLOSCOPES

Manufacturer	Model/price	Sample rate (Msamples/s)/ Vertical resolution (bits)	Repetitive/ single-shot bandwidth (MHz)[1]	Channels/ Record length (samples)	Remarks
Gould Instrument Systems Inc. 8333 Rockside Rd. Valley View, OH 44125 (216) 328-7000	450/$2490	100/8	50/20	2/512 per ch.	Same as Model 420.
	465/$2590	200/8	100/50	2/512 per ch.	Same as Model 420.
	475/$2690	200/8	200/50	2/512 per ch.	Same as Model 420.
	500/$3990	200/8	200/50	2/512 per ch.	Standard automatic measurements; IEEE-488.2; color display; plotter opt.
	1602/$4395	20 (1-ch. oper.)/8	20/7	2/10k per ch.	Opt. automatic measurements, IEEE-488, serial interface, 4-color plotter; DRO recorder.
	4062/$4990	400 (1-ch. oper.)/8	150/150	2/512 per ch.	Automatic measurements; color or thermal plotter, IEEE-488, serial interface opt.
	1604/$5215	20 (2-ch. oper.)/8	20/7	4/10k per ch.	Same as Model 1602.
	4066/$5800	400 (1-ch. oper.)/8	150/150	2/512 per ch.	Same as Model 4062 plus live FFT, math, x-y, scaling measurements.
	4162/$6935	100/8	150/150	4/50k per ch.*	Automatic measurements; IEEE-488.2; serial interface; color or thermal plotter opt. *2-ch. limit sensitivity.
	4064/$6990	400 (2-ch. oper.)/8	150/150	4/512 per ch.	Same as Model 4062.
	4164/$6990	100/8	150/50	4/50k per ch.	Same as Model 4162.
	DataSYS 730/ $6990	100/8	150/50	4/50k per ch.*	Same as Model 4062/4162; opt. hard or floppy disk, extensive analysis; mono display. *2-ch. limit sensitivity.
	DataSYS 750/ $7500	100/8	150/50	4/50k per ch.	Same as DataSYS 730.
	4068/$7700	400 (2-ch. oper.)/8	150/150	4/512 per ch.	Same as Model 4066.
	DataSYS 720/ $7990	100/8	150/50	4/50k per ch.*	Same as DataSYS 730 with color display. *2-ch. limit sensitivity.
	1624/$8050	20 (2-ch. oper.)/8	20/7*	4/10k per ch.	Same as Model 1602 plus 4-ch. differential inputs. *20/3 differential.
	DataSYS 740/ $8500	100/8	150/50	4/50k per ch.	Same as DataSYS 730 with color display.
	4090/$8950	800 (1-ch. oper.)/8	200/200	2/1k per ch.*	Same as Model 4072A. *2 k on 1 ch.
	4072A/$9050	400/8	200/200	2/1k per ch.	Dual timebase; automatic measurements; IEEE-488, serial interface; 4-color plotter opt.
	4092/$9950	800/8	200/200	2/2k per ch.	Same as Model 4072A.
	2608/$9990	20/8	7/7	4/10k per ch.	Same as Model 1602. Std. 8-ch. isolated inputs.
	4074A/$10,550	400/8	200/200	4/1k per ch.	Same as Model 4072A.
	4094A/$10,950	800 (2-ch. oper.)/8	200/200	4/1k per ch.*	Same as Model 4072A. *2 k/ch. on 2-ch oper.
	4096/$10,950	1600 (1-ch. oper.)/8	200/200	2/2k per ch.	Same as Model 4072A.
Hameq Inc. 1939 Plaza Real Oceanside, CA 92056 (800) 247-1241 (619) 630-4080	HM205-3/ $1120	20/8	20/2	2/2k	Analog mode; component tester; plotter output, PC-based analysis software, and IEEE-488 opt.
	HM1007/ $1988	40/8	40/4	2/2k per ch.	Includes 2 reference memories; battery memory back-up; dot joiner; component tester; plotter, IEEE-488, RS-232 opt.
Hewlett-Packard Co. Direct Marketing Org. P.O. Box 58059 MS 51L-SJ Santa Clara, CA 95051-8059 (800) 452-4844	54600B/$2495	20/8	100/2	2/4k per ch.	General-purpose troubleshooting scope with real-time vector display and knob-driven controls; FFT and pass/fail testing opt.
	54601B/$2895	20/8	100/2	4 (2+2)/ 4k per ch.	Same as 54600B.
	54602B/$3250	20/8	150/2	4 (2+2)/4k per ch.	Same as 54600B.

ACCELERATE YOUR TIME TO MARKET



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- Fully isolated outputs
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READER SERVICE 102

DIGITAL STORAGE OSCILLOSCOPES

Manufacturer	Model/price	Sample rate (Msamples/s)/ Vertical resolution (bits)	Repetitive/ single-shot bandwidth (MHz)[1]	Channels/ Record length (samples)	Remarks
Hewlett-Packard Co. Direct Marketing Org. P.O. Box 58059 MS 51L-SJ Santa Clara, CA 95051-8059 (800) 452-4844	54501A/$4725	10/8	100/1	4 (2+2)/4k per ch.	—
	54610B/$4995	20/8	500/2	2/4k per ch.	High-frequency general-purpose troubleshooting scope with same features as 54600B; includes trigger view.
	54503A/$6430	20/8	500/2	4/1K per ch.	—
	54504A/$6880	200/8	400/50	2/2k per ch.	—
	E1426A/$7950	20/8	500/2	4/1k per ch.	2-slot, C-size VXI module; 2-ch. in single-shot mode.
	54502A/$8930	400/6	400/100	2/2k per ch.	—
	54520A/$9500	500/8	500/125	2/32k per ch.	—
	54510B/ $11,950	1000/8	300/250	2/8k per ch.	—
	E1428A/ $12,950	1000/8	250/250	2/32k per ch.	1-slot, C-size VXI module.
	54522A/ $13,500	2000/8	500/500	2/32k per ch.	—
	54540A/ $15,000	1000 (2-ch. oper.)/8	500/250	4/32k per ch.	—
	54512B/ $17,990	1000/8	300/250	4/8k per ch.	—
	54542A/ $21,000	2000/8	500/500	4/32k per ch.	—
	54100D/ $22,900	40/7 (10 with averaging)	1000/4	2/1k	Advanced logic trigger and second trigger input.
	54110D/ $24,900	40/7 (10 with averaging)	1000/4	2/1k per ch.	Same as 54100D with color display.
	54121T/ $31,600	N.A./12 (14 with averaging)	20 GHz/ N.A.	4/1k per ch.	Sequential sampling only.
	54122T/ $33,900	N.A./12 (14 with averaging)	12.4 GHz/ N.A.	4/1k per ch.	Sequential sampling only.
	54710D/ $36,000*	4000/8	N.A./2 GHz	1-4/128k	Modular 2-slot single-shot scope. *Average system price.
	54123T/ $37,900	N.A./12 (14 with averaging)	34 GHz/ N.A.	4/1k per ch.	Sequential sampling only.
	54124T/ $46,200	N.A./12 (14 with averaging)	50 GHz/ N.A.	4/1k per ch.	Sequential sampling only.
	54720A/ $52,000*	8000/8	N.A./1.5 GHz	1-8/64k	Modular 4-slot single-shot scope. *Average system price.
	54720D/ $55,000*	8000/8	N.A./2 GHz	1-8/256k	Modular 4-slot single-shot scope. *Average system price.
	16532A/$9165	1000/8	250/250	2-20/8k	2-ch. card for use with HP 16500B mainframe ($8800); can be triggered by logic analyzer module.
Hitachi Denshi America Ltd. 371 Van Ness Way Suite 120 Torrance, CA 90501 (310) 328-6116	VC-5025/$995	20/6	20/10	2/128 bytes	Portable DMM/DSO; AC/DC current measurements; Ax+B linearization; 8-digit counter-timer; true RMS; RS-232 output.
	VC-6023/ $2075	20/8	20/5	2/2k	Cursor measurements; RS-232, plotter output.
	VC-6024/ $2410	20/8	50/5	2/2k	Same as VC-6023.
	VC-6025A/ $3055	20/8	50/5	2/2k	Dual timebase; RS-232 output.
	VC-5430/ $3495	30/8	50/25	2/2k	Portable; color thin-film transistor LCD display; RS-232 output.

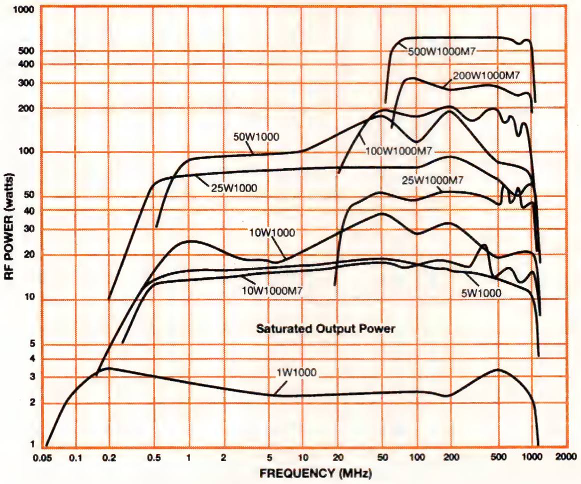
When it gets lonely out there at 1 GHz, you'll be glad you have all this power.

The only amplifier that can deliver 500 watts through that balky decade from 100 to 1,000 MHz is our new Model 500W1000M7. That's the majestic one on the left, with the front-panel bi-directional power meter, ALC, and a bagful of other controls that will let you actually *enjoy* automatic sweep testing in your lab.

The 500W1000M7 presently heads our well-known "W" Series of all-solid-state linear amplifiers that cover four crucial decades of bandwidth from 100 kHz to 1 GHz. Today, you may need only 1 watt (the little portable on the top), or 5, or 10, or 25, or 50, or even 100 or 200 watts *minimum*—all with that fantastic bandwidth instantly available without tuning or bandswitching—a combination of power and bandwidth that's comforting when you work the outer reaches of the rf spectrum. Wherever your power requirements are today, they're sure to go up. And one of these days you're going to want a 500W1000M7.

The "W" Series is part of a complete line of AR amplifiers offering rf power up to 10 kilowatts for rf susceptibility testing, nmr spectroscopy, plasma/fusion research, and a host of other test situations that demand rf power of unconditional stability—immunity to even the worst-case load mismatch, shorted or open cable, wild swings of VSWR—with no fear of oscillation, foldback, or system shutdown.

You might learn a lot from our free booklet, "Guide to Broadband Power Amplifiers." Send for a copy. Or call our toll-free number (800-933-8181), which will connect you directly to one of our applications engineers.



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Souderton, PA 18964-9990 USA
TEL 215-723-8181 • FAX 215-723-5688

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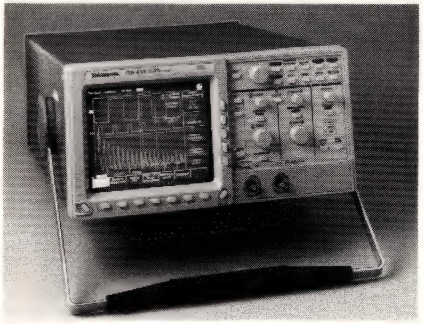
READER SERVICE 142

5351

▼ 150-MHZ DSO HAS 1.5% VERTICAL ACCURACY

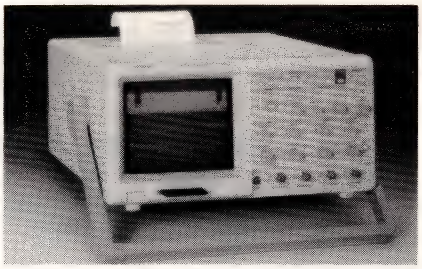


The TDS 410 is an economical digital oscilloscope that features a 150-MHz bandwidth and 100-Msample/s sampling rate, with 1.5% vertical accuracy and 1-mV/division precision. Standard record length is 15 ksamples/channel, expandable to 60 ksamples. Automatic test setups, 25 automated measurements, pass/fail templates, and an intuitive icon-based interface make it easy to measure and verify complex signals. To ensure fast measurement, display, and analysis capability, the TDS 410 uses a Motorola 68020, a custom display processor, and a proprietary digital signal processor. An optional Math Pack adds fast Fourier transform, integration, and differentiation functions. The TDS 410 costs $4950, with delivery in approximately four weeks.

Tektronix Inc.
Test and Measurement Group
P.O. Box 1520
Pittsfield, MA 01202
(800) 426-2200, ext. 282
▶ CIRCLE 753

▼ 4-CHANNEL DSO BOASTS 2-MBYTE/CHANNEL MEMORY

The four-channel VC-7124 digital storage oscilloscope features an acquisition memory of 2 Mbytes per channel. The deep memory allows users to capture waveforms up to 20 ms long at the unit's full sampling rate of 100 Msamples/s. Bandwidth of the scope is 150 MHz. The memory can be partitioned to permit continuous capture of up to 2000 waveforms with no more than 1 μs dead time between them. Multiple real-time magnification windows help users observe details within the long records. Features include a PCMCIA card slot, go/no-go mask testing, a built-in thermal printer, and a video trigger. The VC-7124 costs $12,500. Delivery is within 10 weeks.



Hitachi Denshi America Ltd.
371 Van Ness Way
Suite 120
Torrance, CA 90501
(310) 328-6116
▶ CIRCLE 754

DIGITAL STORAGE OSCILLOSCOPES

Manufacturer	Model/price	Sample rate (Msamples/s)/ Vertical resolution (bits)	Repetitive/ single-shot bandwidth (MHz)[1]	Channels/ Record length (samples)	Remarks
Hitachi Denshi America Ltd. 371 Van Ness Way Suite 120 Torrance, CA 90501 (310) 328-6116	VC-6045A/ $3535	40/8	100/5	2/4k	Dual timebase; RS-232 output.
	VC-7102/ $5275	100/8	150/25	2/8k per ch.	Automatic setup; built-in printer; IEEE-488, RS-232; PCMCIA card slot.
	VC-6145/ $5410	100 (1-ch. oper.)/8	100/5	4/4k	Cursor measurements; RS-232, plotter outputs.
	VC-7104/ $6495	100/8	150/25	4/8k	Same as VC-7102.
	VC-7124/ $12,500	100/8	150/25	4/4M per ch.	Built-in printer; IEEE-488, RS-232; PCMCIA card slot.
Kikusui International Corp. 1980 Orizaba Ave. Signal Hill, CA 90804 (800) 545-8784 (310) 986-1677	COR5521u/ $1495	20/8	20/5	2/4k per ch.	Includes analog mode; IEEE-488, RS-232C opt.
	COR5541u/ $1595	20/8	40/5	2/4k per ch.	Same as COR5521u.
	COR5561u/ $1795	20/8	60/5	2/4k per ch.	Same as COR5521u.
	COR5501u/ $1995	20/8	100/5	2/4k per ch.	Same as COR5521u.
	COR5502u/ $2499	100/8	100/25	2/4k per ch.	Same as COR5521u.
Leader Instruments Co. 380 Oser Ave. Hauppague, NY 11788 (800) 645-5104 (516) 231-6900	LDC-100/$925	3/6	0.2/0.2	1/256	Stores 3 waveforms; includes DMM; hand-held; LCD.
	300/$1995	30/7	10/3	2/1.8k per ch.	Includes DMM, logic analyzer, data logger; LCD.
	LBO-5825/ $2450	5/8	0.5/0.5	2/1k per ch.	35-MHz analog mode.
	3060D/$3395	40/8	100/10	2/2k per ch.	100-MHz analog mode; auto measurements; IEEE-488.
	3100A/$3695	40/8 (1-ch. oper.)	10/10	2/2k per ch.	60-MHz analog mode; cursor readouts; IEEE-488.

▼ RF SIGNAL GENERATORS STORE TEST SEQUENCES

Three economical signal generators target high-volume RF applications, such as cordless phones, pagers, and low-cost two-way radios. Frequency coverage starts at 100 kHz and ranges to 1 GHz (HP 8648A), 2 GHz (HP 8648B), and 3.2 GHz (HP 8648C). The instruments contain 300 storage registers and up to 10 user-definable test sequences that can be accessed from the front panel or from a remote keypad. The keypad is a mouse-like device that simplifies operation and saves space on the test bench. Residual FM for hum and noise measurements is less than 7 Hz up to 1 GHz, less than 14 Hz up to 2 GHz, and less than 28 Hz up to 3.2 GHz. Power-level accuracy is ±1.0 dB at −127 dBm. The HP 8648A costs $5865, the HP 8648B $7665, and the HP 8648C $9165. Delivery is in four weeks.

Hewlett-Packard Co.
Direct Marketing Org.
P.O. Box 58059
MS51L-SJ
Santa Clara, CA 95051-8059
(800) 452-4844, ext. 8023
▶CIRCLE 755

▼ BOUNDARY-SCAN CAD TOOL INCLUDES BSDL EDITOR

A comprehensive automated system that supports device-level implementation of boundary-scan architecture is now included in the ATTDFT for Circuit Design product family. Called BCAD1, the system contains a sophisticated graphical Boundary-Scan Description Editor for creating and editing boundary-scan description language (BSDL) files. Users first enter functional-level specifications. Then the system automatically generates a BDSL file, ensuring that the scan logic is defect-free. BCAD1 also generates conformance vectors to verify that an implementation complies with the boundary-scan standard. Using the same graphical interface, the system accepts the BSDL file as its input and automatically creates the vectors. The vectors also ensure that the boundary-scan implementation matches the BSDL description and provide high fault coverage for the device's boundary-scan logic. BCAD1 runs on Sun Sparcstations under Unix 4.1 or higher with a minimum memory of 32 Mbytes. Disk space required depends on the circuit under test. The system is available immediately for $16,000 per CPU license.

AT&T Design Automation
Room 2B-247
1247 S. Cedar Crest Blvd.
Allentown, PA 18103-6025
(800) 875-6590
▶CIRCLE 756

DIGITAL STORAGE OSCILLOSCOPES

Manufacturer	Model/price	Sample rate (Msamples/s)/ Vertical resolution (bits)	Repetitive/ single-shot bandwidth (MHz)[1]	Channels/ Record length (samples)	Remarks
LeCroy Corp. 700 Chestnut Ridge Rd. Chestnut Ridge, NY 10977-6499 (800) 553-2769 (914) 425-2000	LS140/$3990	200/8	100/80	4/2k	Floppy drive std.; 20-k memory, 100-Mbyte hard drive, $795; fax modem, IEEE-488, network card opt.
	9310/$4990	100/8	300/40	2/10k	All 9300-series scopes have opt. floppy drive, high-resoution graphics printer, PCMCIA slot, advanced math, and FFT.
	9304/$5990	100/8	300/40	4/10k	See Model 9310.
	9310M/$5990	100/8	300/40	2/50k	See Model 9310.
	9304M/$6990	100/8	300/40	4/50k	See Model 9310.
	9320/$7490	40/8	1000/16	2/5k	Sampling scope; see Model 9310.
	9314/$7860	100/8	300/40	4/10k	See Model 9310.
	9361/$8990	2500/8	300/300	2/500	Opt. memory to 25k; see Model 9310.
	9450A/$9290	400/8	300/160	2/50k	—
	9314M/$9440	100/8	300/40	4/50k	See Model 9310.
	9350/$9490	500/8	500/200	2/25k	1 Gsample/s and 50-k memory in 1-ch. operation; see Model 9310.
	9310L/$10,490	100/8	300/40	2/1M	See Model 9310.
	9350M/ $11,490	500/8	500/200	2/100k	1 Gsample/s and 250-k memory in 1-ch. operation; see Model 9310.
	9324/$11,490	40/8	1000/16	4/5k	Sampling scope; see Model 9310.
	9360/$12,490	5000/8	600/600	2/500	Opt. memory to 25k; See Mode 9310.
	9354/$13,990	500/8	500/200	4/25k	2 Gsamples/s and 100-k memory in 1-ch. operation; see Model 9310.
	9314L/$15,740	100/8	300/40	4/1M	See Model 9310.
	9350L/$16,490	500/8	500/200	2/1M	1 Gsample/s and 4-M memory in 1-ch. operation; see Model 9310.

DIGITAL STORAGE OSCILLOSCOPES

Manufacturer	Model/price	Sample rate (Msamples/s)/ Vertical resolution (bits)	Repetitive/ single-shot bandwidth (MHz)^1	Channels/ Record length (samples)	Remarks
LeCroy Corp. 700 Chestnut Ridge Rd. Chestnut Ridge, NY 10977-6499 (800) 553-2769 (914) 425-2000	9354M/ $16,490	500/8	500/200	4/100k	2 Gsamples/s and 500-k memory in 1-ch. operation; see Model 9310.
	9430/$19,940	100/10	150/40	2/50k	—
	9354L/$24,490	500/8	500/200	4/2M	2 Gsamples/s and 8-M memory in 1-ch. operation; see Model 9310.
	7200AM-7262/ $24,990	40/10	4000/16	2/10k	Sampling scope, TDR opt.; all 7200A-series scopes have hard drive, floppy drive, advanced processing functions, color display, and SCSI port available.
	7200AM-7234/ $32,025	200/8	500/80	4/50k	Modular; second 7234 plug-in adds 4 channels ($19,425); see Model 7200AM-7262.
	7200AM-7242B/$34,545	1000/8	500/400	2/200k	2 Gsamples/s in 1-ch. operation; modular; second 7242B plug-in adds 2 channels ($21,945); see Model 7200AM-7262.
	7200AM-7234L1/ $35,175	200/8	500/80	4/200k	1M memory in 1-ch. operation, see Model 7200AM-7262
	7200AM-7242BL1/ $37,695	1000/8	500/400	2/1M	2 Gsamples/s in 1-ch. operation; see Model 7200AM-7262.
Nicolet Instrument Corp. 5225 Verona Rd. Madison, WI 53711 (800) 356-8088 (608) 271-3333	310/$5995	1/12*	0.4/0.4	2/4k per ch.	DOS disk drive; IEEE-488; RS-232. *Differential inputs.
	Pro 50/ $11,490	200/8	100/100	2/64k per ch.	DOS disk drive; 128-Mbyte optical drive; math functions; IEEE-488; RS-232; Basic-like programming; 256-k/ch. memory opt.
	Pro 10/ $11,990	1/12*	0.5/0.5	2/64k per ch.	Same as Pro 50. *Differential inputs.
	Pro 60/ $16,490	200/8	100/100	4/64k per ch.	Same as Pro 50.
	Pro 20/ $16,990	1/12*	0.5/0.5	4/64k per ch.	Same as Pro 50. *Differential inputs.
	Pro 30/ $17,990	10/12*	5/5	2/256k per ch.	Same as Pro 50 except 1-Mbyte/ch. opt. memory. *Diffential inputs.
	Pro 32/ $19,990	20/12*	10/10	2/256k per ch.	Same as Pro 30. *Diffential inputs.
	Pro 34/ $19,990	5/14*	2.5/2.5	2/256k per ch.	Same as Pro 30. *Differential inputs.
	Pro 90/ $20,990	10/12 200/8*	5/5 100/100	4/64k per ch.	Same features as Pro 50. *2 ch. each, with differential inputs for 12 bits.
	Pro 40/ $24,990	10/12*	5/5	4/256k per ch.	Same as Pro 30.
	Pro 92/ $26,990	20/12 200/8*	10/10 100/100	4/256k per ch.	Math functions; DOS disk drive; 128-Mbyte optical drive; IEEE-488; RS-232; Basic-like programming. *2 ch. each, with differential inputs for 12 bits.
	Pro 42/ $28,990	20/12*	10/10	4/256k per ch.	Same as Pro 30. *Differential inputs.
	Pro 44/ $28,990	5/14*	2.5/2.5	4/256k per ch.	Same as Pro 30. *Differential inputs.
Panasonic Factory Automation 9377 W. Grand Ave. Franklin Park, IL 60131 (708) 288-4471	VP-5710A/ $3995	20/8	100/8	4/64k	100-MHz analog mode; IEEE-488 std.
	VP-5720A/ $5900	40/8	100/16	2/8k per ch.	50-MHz dual-trace analog mode; IEEE-488 std.
	VP-5741A/ $8900	100/8	100/35	2/10k	100-MHz analog mode; IEEE-488 std.
	VP-5750A/ $9900	200/8	100/70	2/80k	IEEE-488 std.
	VP-5760A/ $12,000	100/10	100/35	2/10k	EIA and CCIR scaling; pedestal clamp; IEEE-488 std.

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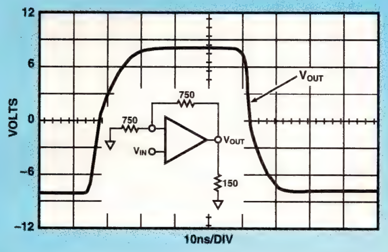

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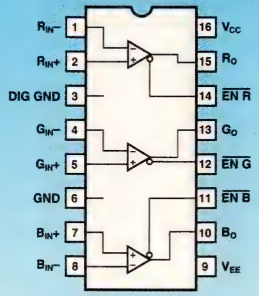

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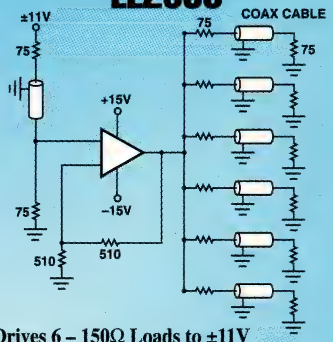

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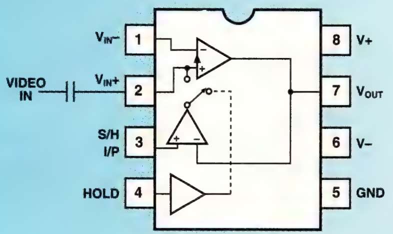

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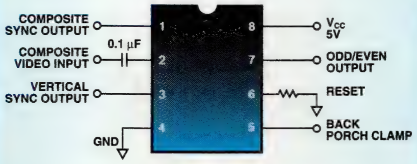

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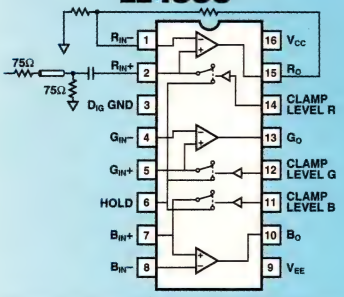

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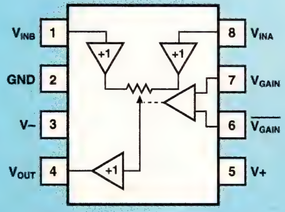

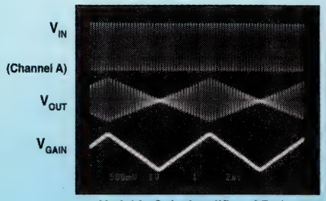

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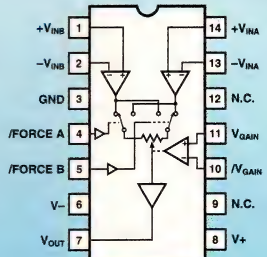

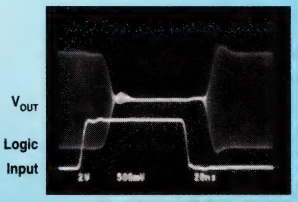

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DIGITAL STORAGE OSCILLOSCOPES

Manufacturer	Model/price	Sample rate (Msamples/s)/ Vertical resolution (bits)	Repetitive/ single-shot bandwidth (MHz)[1]	Channels/ Record length (samples)	Remarks
H.C. Protek Inc. P.O. Box 59 Norwood, NJ 07658 (201) 767-7242	P-3820/$975	20/8	2.5/2.5	2/2k per ch.	15-waveform memory; RS-232 interface.
	P-3850/$1350	50/8	5/5	2/2k per ch.	Built-in DMM and logic analyzer; memory for 15 waveforms, 15 DMM readings, and 15 logic analyzer states; RS-232 interface.
	P-2820/$1490	20/8	2.5/2.5	2/2k per ch.	20-MHz analog mode; cursor measurements.
	P-2840/$1895	20/8	2.5/2.5	2/2 k per ch.	40-MHz analog mode; cursor measurements.
Tektronix Inc. Test and Measurement Group P.O. Box 1520 Pittsfield, MA 01202 (800) 426-2200	TDS 310/ $2295	200/8	50/50	2/1k per ch.	Graphical user interface; automatic setup and measurements; IEEE-488, RS-232C, centronics port opt.; thermal printer opt.
	2201/$2295	10/8	20*/1	2/2k per ch.	*Analog mode. Single timebase; RS-232C opt.
	222A/$2550	10/8	10/1	2/512	Hand-held, battery-powered; RS-232C; inputs floatable to 400 V.
	2212/$2695	20/8	60*/2	2/4k per ch.	*Analog mode. Single timebase, IEEE-488, RS-232C, Centronics opt.; 128-k memory opt.
	224/$2750	10/8	60/1	2/512	Same as Model 222A except floatable to 850 V.
	TDS 320/ $2895	500/8	100/100	2/1k per ch.	Same as Model 310.
	222PS/$2950	10/8	10/1	2/512	Same as Model 224.
	TDS 350/ $3995	1000/8	200/200	2/1k per ch.	Same as Model 310.
	2214/$4195	16/8	20*/1	4/16k per ch.	*Analog mode. Single timebase; RS-232C.
	2221A/$4695	100/8	100/10	2/1k or 4k	Combination analog and digital; single timebase; IEEE-488, RS-232C opt.
	TDS 410/ $4950	100/8-12*	150/40	2/15k	*Includes high-resolution mode. 60-k memory opt.; graphical user interface; RS-232C, Centronics, FFT math, opt.
	2232/$5595	100/8	100/10	2/1k or 4k	Same as Model 2221A with dual timebase.
	TDS 420/ $6295	100/8-12*	150/40	4/15 k	Same as TDS 410.
	TDS 460/ $7495	100/8-12*	350/40	4/15k	Same as TDS 410.
	TDS 520A/ $8895	500/8-12*	500/200	2/15k	*Includes high-resolution mode. 50-k memory opt.; graphical user interface; sophisticated triggering.
	TDS 524A/ $10,900	500/8-12*	500/200	4/15k	*Includes high-resolution mode. Same as TDS 520A, with color display.
	TDS 620A/ $11,895	2000/8-12*	500/500	2/2k	*Includes high-resolution mode. Graphical user interface; sophisticated triggering.
	TDS 540A/ $14,340	1000/8-12*	500/400	4/15k	*Include high-resolution mode. 50-k memory opt.; same as TDS 520A.
	TDS 544A/ $16,790	1000/8-12*	500/400	4/15k	*Includes high-resolution mode. 50-k memory opt.; same as TDS 524A.
	11402A/ $17,500	20/10*	1000/N.A.	to 8/10k	*14 with averaging. Bandwidth, channel count depend on amplifier modules selected; extensive measurement capability; color display.
	TDS 640A/ $17,550	2000/8-12*	500/500	4/2k	*Includes high-resolution mode. Same as TDS 520A.
	TDS 644A/ $19,895	2000/8-12*	500/500	4/2k	*Includes high-resolution mode. Graphical user interface; sophisticated triggering, color display.
	TDS 820/ $19,900	0.050/14	8000/N.A.	2/15k	2-ps delta time and 0.4-ps timing resolution; graphical user interface.
	11403A/ $19,900	20/10*	3000/N.S.	to 8/10k	*14 with averaging. Same as 11402A.
	CSA 404/ $22,000	20/10	3000/5	to 12*/10k	*With additional modules. Statistical database; automated mask testing, including telecommunications; eye-pattern analysis; single-shot time-interval measurement with 200-ps resolution.

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Hameg Instruments
1939 Plaza Real
Oceanside, CA 92056
(800) 247-1241 or (619) 630-4080
▶ CIRCLE 757

▼ HANDHELD UNITS ANALYZE POWER HARMONICS

Two new handheld instruments are designed to troubleshoot power-harmonics problems and manage electrical power usage. With a single button press, the Model 40 power-harmonics meter and Model 41 power-harmonics analyzer allow users to view the signal in one of three ways: as a waveform, in a bar graph showing the levels of harmonics and the percentage of each, and as a numeric value. The units measure voltage, current, frequency, and power. They also supply power factor, crest factor, and total harmonic distortion. Furthermore, the Model 41 measures K-VAR corrections and adds storage of eight measurement sets, an RS-232 serial interface, and three extra displays for additional information. The Model 40 costs $1200, and the Model 41 goes for $1700.

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Everett, WA 98206
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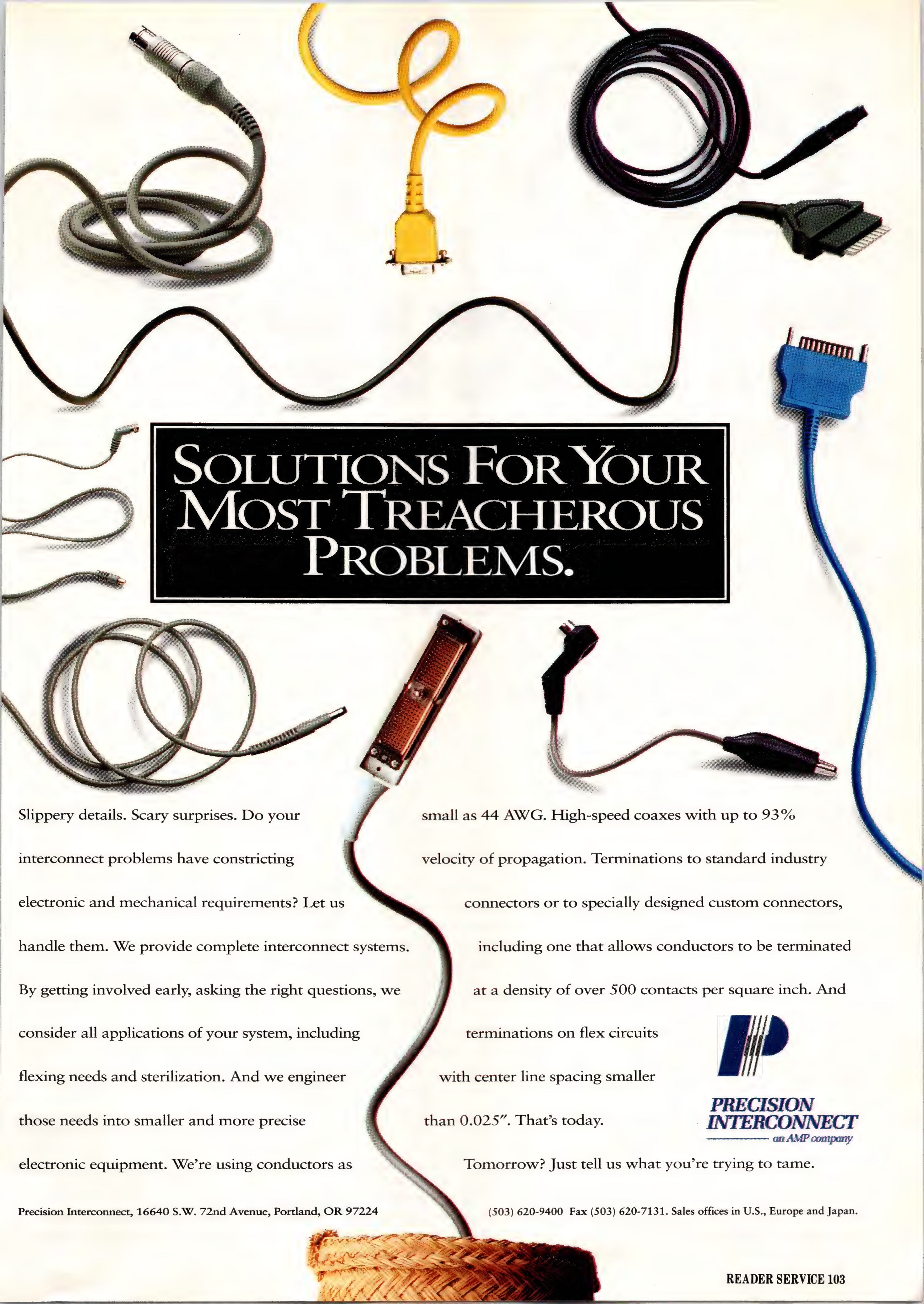
Omega Engineering Inc.
1 Omega Dr.
P.O. Box 4047
Stamford, CT 06907-4047
(203) 359-1660
▶ CIRCLE 759

DIGITAL STORAGE OSCILLOSCOPES

Manufacturer	Model/price	Sample rate (Msamples/s)/ Vertical resolution (bits)	Repetitive/ single-shot bandwidth (MHz)[1]	Channels/ Record length (samples)	Remarks
Tektronix Inc. Test and Measurement Group P.O. Box 1520 Pittsfield, MA 01202 (800) 426-2200	CSA 803A/ $25,150	0.2/8	50 GHz/ N.S.	to 4*/5k	*With additional modules. Same as CSA 404 with TDR and 10-GHz triggering.
	11801B/ $26,500	0.2/8*	3-50 GHz/ N.A.	to 136/5k	—
	DSA 601A/ $27,000	1000/8*	1000/500	8*/20k	*14 bits with averaging; 2 ch. in single-shot mode. Bandwidth, channel count depend on amplifier selected; extensive signal processing and analysis capability.
	TDS684A/ $29,495	5000/8	N.A./1000	4/15k per ch.	Slew-rate and setup-and-hold trigger; 3.5-in. DOS drive; color display; 1-GHz probe $1,395 (four for $5,195).
	DSA 602A/ $32,600	2000/8*	1000/1000	8*/32k	*14 bits with averaging; 4 ch. in single-shot mode. Same as DSA601A.
Yokogawa Corp. of America 2 Dart Rd. Newnan, GA 30265 (404) 253-7000	DL1100/$3750	25/8	100/8	2/32k per ch.	Automated measurements; printer, memory card opt.
	DL1200A/ $4995	100 (1-ch. oper.)/8	100/40	4/32k per ch.	Automated measurements; printer, memory card opt.
	DL1300A/ $5995	100/8	100/40	4/64k per ch.	128-ksample memory for 2-ch. oper.; 2-ch. go/no-go testing; 21 automated measurements; printer, memory card opt.
	DL2100/ $13,500	200/8	300/80	2/128k per ch.	Waveform analysis, printer, memory card opt.
	DL3100/ $21,000	25/12	10/10	2/256k per ch.	Waveform analysis, memory expansion opt.; differential inputs, printer.

1. Manufacturers specify single-shot bandwidth differently, depending on what type of interpolation or waveform reconstruction technique, if any, the instrument uses. Typical specifications run from two points per sampled frequency (the minimum required by Nyquist's theorem) to 10 points per sampled frequency if no interpolation is used.



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A SPECIAL EDITORIAL FEATURE

PIPS

POWER • INTERCONNECTIONS • PASSIVES • SWITCHES • RELAYS

ELECTRONIC DESIGN

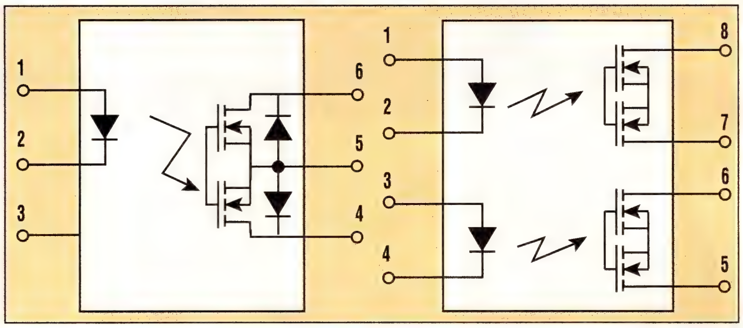
High I/O Isolation In LED-MOS Relays Opens Up Application Horizons

Optical isolation and elimination of zero-crossover problems lend versatility.

BY DOUGLAS J. LIONETTI

Aromat Corp., Precision Components Group, 629 Central Ave., New Providence, NJ 07974; (908) 464-3550.

With the advent of semiconductors has come a parade of solid-state switching devices. During the last couple of decades, SCRs, triacs, and solid-state relays (SSRs) have actively competed with "old reliable"—the electromechanical relay (EMR)—which has been around for over 100 years. Although SSRs have taken over some EMR applications, there was one parameter that they just couldn't beat: The high I/O isolation inherent in every EMR. In addition, conventional SSRs suffer from the problems associated with their zero-crossover characteristic.



1. High I/O isolation in a LED-MOS relay is achieved by means of an optical link between the input and output. An ac/dc relay with a Form A contact configuration is on the left; two ac/dc Form A contacts are on the right.

In recent years, a different type of solid-state relay solved both of these problems by combining optoelectronic and MOS technologies. To make sure that users don't confuse these new SSRs with their conventional counterparts, various manufacturers have assigned names to them. While a very descriptive name for them could be LED-MOS relays, Aromat, for one, calls them PhotoMOS relays.

To clear the fog surrounding the relatively new relay technology, this article will briefly describe the basic operating principle of LED-MOS relays. This will be followed by a summary of available packages and their current, voltage, and power capabilities. Finally, several applications will be described.

As a signal is applied to the LED input, current begins to flow through the LED, which emits light. The emitted light falls upon a photoelectric element (a solar cell) that's mounted beneath the LED. The photoelectric element produces a voltage proportional to the amount of received light. That voltage is applied to a control circuit which charges the MOSFET gate on the output side. When the MOSFET gate voltage supplied by the photoelectric element reaches its "trip" value, the MOSFET switches to its conducting state and the load is turned on.

As can be readily appreciated even from this simplistic description, a LED-MOS relay is a solid-state relay with an important difference: It offers very high I/O-isolation characteristics and, unlike SSRs, it doesn't suffer from the zero-crossover problem. There's no physical connection between the LED input and the unit's output terminals *(Fig. 1)*. The "connection" is a light beam produced by the LED in response to a relatively low-level input signal.

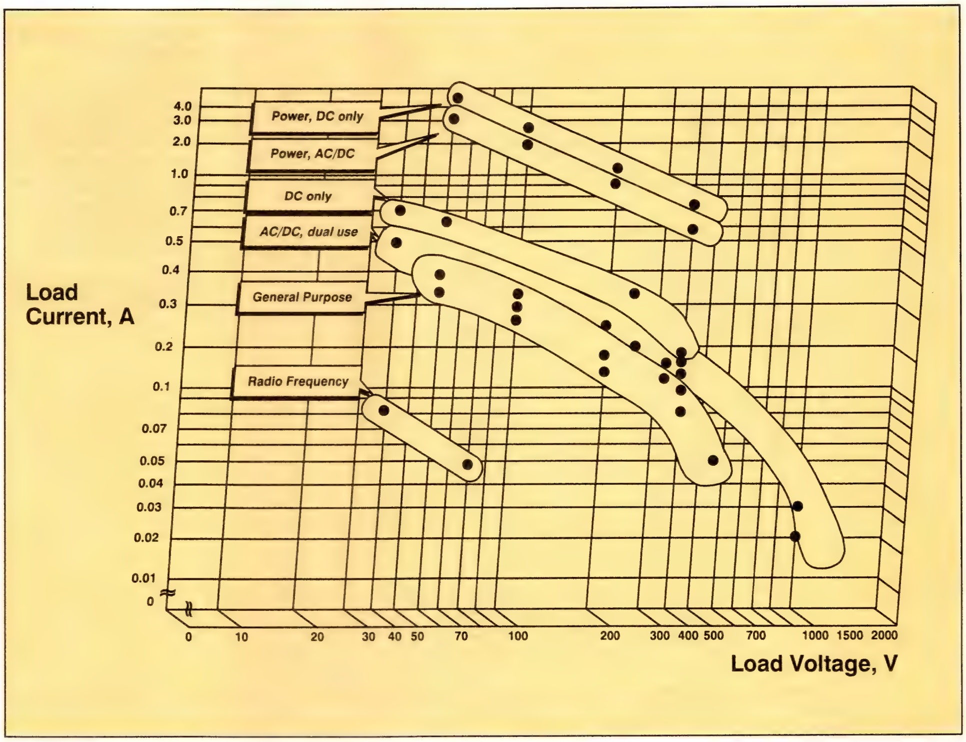
In addition to the isolation benefits, the use of MOSFET switching provides even more advantages. The relays offer low and stable on-resistance down to 0.05 Ω and high I/O isolation of up to 5000 V. Their life span is infinite, unless they're misused. Control of signals down to 0.05 A at 80 V is possible, although load currents can be as high as 4 A. They operate quickly (0.1 to 2 ms) and with no audible noise. Because there are no moving parts, 100% contact stability is attained with no bounce or chatter. Electrical noise or arcing is eradicated, and the devices meet various domestic and international standards. Again, many of these benefits are the result of the marriage of optical isolation and MOSFET switching.

Though LED-MOS relays can serve as cost-effective replacements for a broad variety of EMRs and SSRs, they're particularly well suited as replacements for reed relays. In this case, they offer the advantages of improved life, higher reliability, greater I/O isolation, smaller size, higher mounting density, and total mounting versatility.

By combining photoelectric and MOSFET technologies, LED-MOS relays offer certain advantages over conventional EMRs and SSRs. Eliminating contact bounce, for instance, means that LED-MOS relays solve the problem of false readings frequently produced by EMRs when used in fast-response circuitry. And, unlike conventional SSRs, LED-MOS relays can switch even low analog and digital signals with little or no distortion because the zero-crossover problem, inherent in SSRs, doesn't exist.

Since their 1992 debut, LED-MOS relays have continuously expanded their packaging diversity and power-handling capability *(Fig. 2)*. While units are available for both dc and ac/dc service, these relays also offer a choice of contact configurations: A (normally open, or NO), or B (normally closed, or NC). For specific applications, units are available with various combinations of these contact configurations in a single package. Or, in some cases, different configurations can be obtained by external wiring.

On the packaging side, LED-MOS relays originally were available only in 6- and 8-pin DIPs and 6- and 8-pin surface-mounted packages. But as small-outline packages (SOPs) become available, LED-MOS relays and their inherent advantages will find their way into many new applications. With the SOP package, users benefit from volumes that are only 25% of a DIP LED-MOS unit, and a 50% smaller footprint when compared with DIPs *(Fig. 3)*.

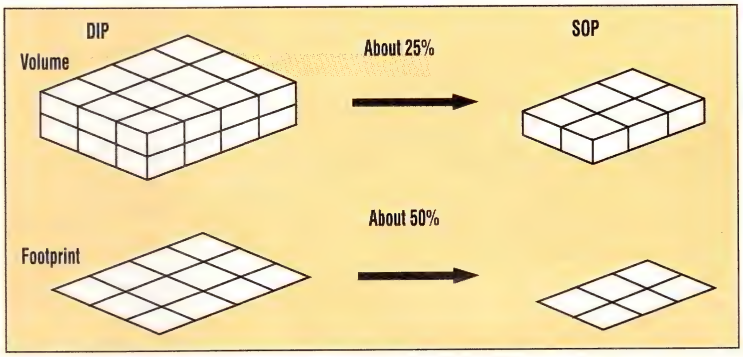


2. A wide range of applications is covered by today's LED-MOS units. Relays with increased capabilities are added at a rapid pace. The figure gives an idea of the breadth of power-handling capabilities available.

Other space-saving packages are the multichannel LED-MOS relays that cut mounting area by over 50% and can switch low-level signals. These units put several relay circuits in the same package. One example configuration is a four-circuit (form A) type that can switch ac or dc continuous currents up to 80 mA per channel (peak load current is 0.3 A) and sustain load voltages up to 400 V. By enclosing four relays in one package, pc-board-area savings of over 50% can be realized *(Fig. 4)*. Applications include a variety of industrial and commercial equipment in telecommunications, control equipment, robots, and those that use reed relays and/or conventional SSRs.

On the power-handling front, power LED-MOS units now offer current ratings ranging from 0.5 to 4 A *(Fig. 2, again)*. These come in 4-pin single in-line packages. Their more important characteristics include very low on-resistances (down to 0.05 Ω) and turn-on times as fast as 0.83 ms. Their standard I/O isolation of 2500 V is typical of conventional EMRs.

Incidentally, that specification of a 2500-V isolation rating for a power LED-MOS relay alludes to a tradeoff that results from the juxtaposition of optical isolation and MOSFET switching. The I/O isolation depends



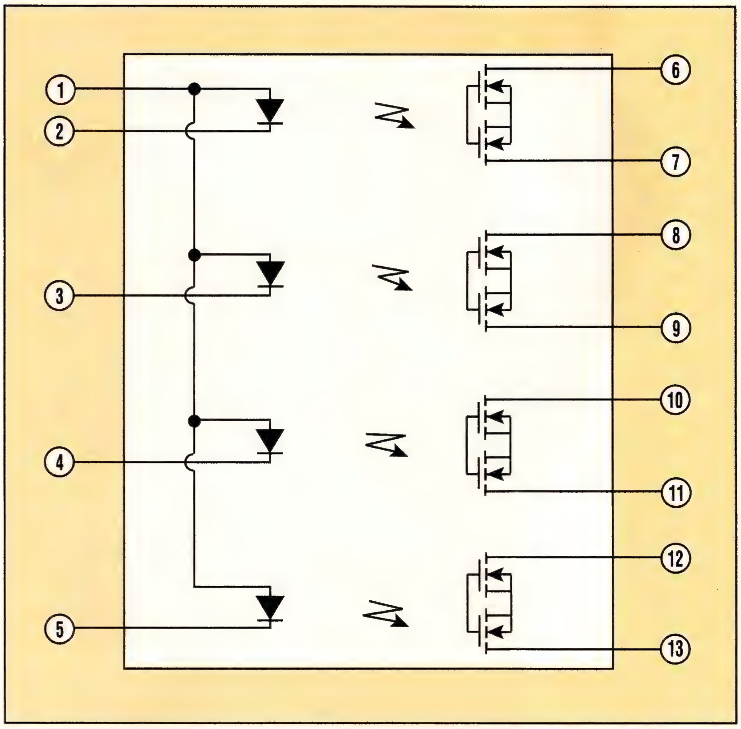
3. With the technology maturing, packaging improvements—size reduction in this case—are fueling the application expansion. The small-outline package (SOP) provides designers with a great deal of density.

on the physical distance between the LED and photosensor that turns the switch on. But the power handling depends on the physical size of the MOSFET die. Hence, for a given package size, a larger die, which handles more power, takes more space and forces closer placement of the optical elements, which lowers isolation from the optimal 5000-V specification.

Equipment and circuit designers have been quick to jump on the LED-MOS bandwagon. Although the technology is only a couple of years old, novel applications continue to evolve almost daily. The LED-MOS guide was developed to help designers get a ballpark idea of their relay choice *(see the table)*. It lists some of the more popular application areas and indicates the general suitability of LED-MOS relays to handle each specific class of applications. When dealing with a similar application, designers can extrapolate the table data to fit his needs.

LED-MOS relays have helped designers solve some unique problems. For one, LED-MOS relays used in the SOP package made it possible for a manufacturer of PCMCIA cards to literally go on-line. In the beginning, these cards gave notebook-PC users ready-to-add expansion memory. But now these cards also can contain a modem for connecting the PC to a phone line. Space and power limitations ruled out conventional EMRs. And conventional SSRs were out because of insufficient I/O isolation and excessive on-resistance and size. LED-MOS relays in standard DIPs and surface-mount packages also were too big. The SOP units were small enough and met the tight phone-line isolation requirements.

Another interesting case was when an instrumentation company, working in process control (typical variables are pressure, temperature, and flow), was developing a system that would give them as much real-



4. Another packaging "trick" that saves board space is to combine four relays in a single in-line (SIL) configuration. In this case, each of the four relays can switch continuous currents of up to 80 mA with load voltages up to 400 V.

LED-MOS RELAY APPLICATION GUIDE

Application		Features	Suitability
Telecommunication	PBX & central office	Surge resistance Mounting density Long life High reliability	Good
	Dial pulse	High speed Make ratio Small bouncing	High
	Line switching	Small size Mounting density High sensitivity Breakdown voltage between I/O	High
Measuring instruments	Scanner	Stability of contact resistance Dynamic contact resistance Low thermal electromotive force High insulation resistance	High
	Board tester	High speed Long life High insulation resistance High reliability	Good
	Automatic meter reading	High sensitivity	High
	Exchange of RF signal	RF characteristics High insulation	Good
Security equipment		No sound Wide load range	High
Computer Audio visual	Exchange of RF	1 to 1.75 GHz 50 to 550 MHz VCR	Unfit
	High-density mounting	Low profile High sensitivity	High
	Interface	Wide load range High insulation	Good
Factory automation	Interface	Noise resistance No sound High sensitivity	High
	Control (motor, heater etc.)	Long life Phase control	Good

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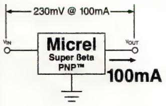
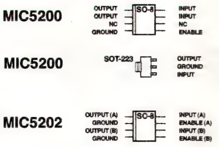
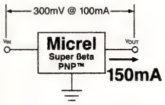


MIC5200/5202

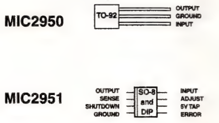
- Guaranteed 100mA output
- 3.3V, 4.5V, 4.75V, and 5.0V fixed
- 230mV drop out at 100mA
- Super βeta PNP™ provides minimum ground current
- MIC5200 Single is available in SO-8 and SOT-223 packages
- MIC5202 Dual is available in SO-8

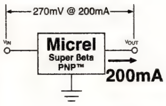




MIC2950/51

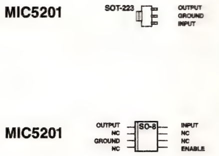
- Guaranteed 150mA output
- 5.0V fixed plus adjustable
- 370mV drop out at 150mA
- Super βeta PNP™ provides minimum ground current
- Available in SO-8 and TO-92 packages

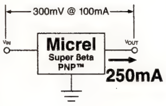




MIC5201

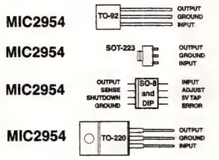
- Guaranteed 200mA output
- 3.3V, 4.5V, 4.75V, and 5.0V fixed
- <400mV drop out at 200mA
- Super βeta PNP™ provides minimum ground current
- Available in SO-8 and SOT-223 packages

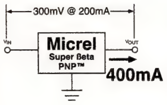




MIC2954

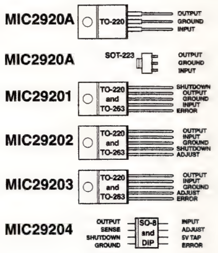
- Guaranteed 250mA output
- 5.0V fixed plus adjustable
- 450mV drop out at 250mA
- Super βeta PNP™ provides minumum ground current
- Available in SO-8 and SOT 223, DIP, TO-220, and TO-92 packages

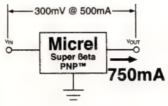




MIC2920A

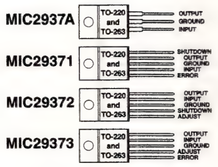
- Guaranteed 400mA output
- 3.3V, 4.85V, 5V, 12V fixed plus adjustable
- <450mV drop out at 400mA
- Super βeta PNP™ provides minimum ground current
- Available in SO-8, DIP, TO-220, and SOT-223 packages

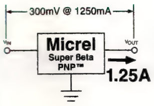




MIC2937A

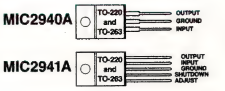
- Guaranteed 750mA output
- 3.3V, 5V, 12V fixed plus adjustable
- 370mV drop out at 750mA
- Super βeta PNP™ provides minimum ground current
- Available in TO-220 and TO-263 packages

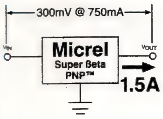




MIC2940A

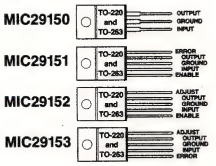
- Guaranteed 1250mA output
- 3.3V, 5V, 12V fixed plus adjustable
- 300mV drop out at 1.25A
- Super βeta PNP™ provides minimum ground current
- Available in TO-220, TO-263, and TO-3 packages

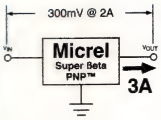




MIC29150

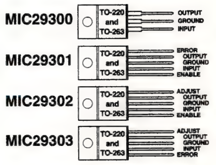
- Guaranteed 1.5A output
- 3.3V, 5V, 12V fixed plus adjustable
- <450mV drop out at 1.5A
- Zero power shutdown mode
- Super βeta PNP™ provides minimum ground current
- Available in TO-220 and TO-263 packages

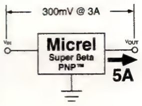




MIC29300

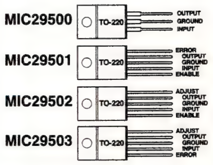
- Guaranteed 3A output
- 3.3V, 5V, 12V fixed plus adjustable
- <450mV drop out at 3A
- Zero power shutdown mode
- Super βeta PNP™ provides minimum ground current
- Available in TO-220 and TO-263 packages

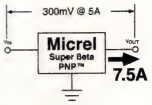




MIC29500

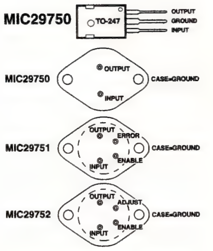
- Guaranteed 5A output
- 3.3V, 5V, 12V fixed plus adjustable
- <450mV drop out at 5A
- Zero power shutdown mode
- Super βeta PNP™ provides minimum ground current
- Available in TO-3 and TO-220 and TO-263 packages (See MIC29750 for TO-3 pinout)

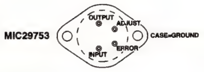


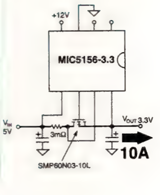


MIC29750

- Guaranteed 7.5A output
- 3.3V, 5V, 12V fixed plus adjustable
- <450mV drop out at 7.5A
- Zero power shutdown mode
- Super βeta PNP™ provides minimum ground current
- Available in TO-3 and TO-247 packages







MIC5156/5157/5158

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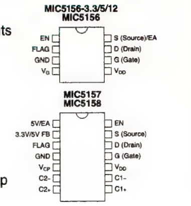

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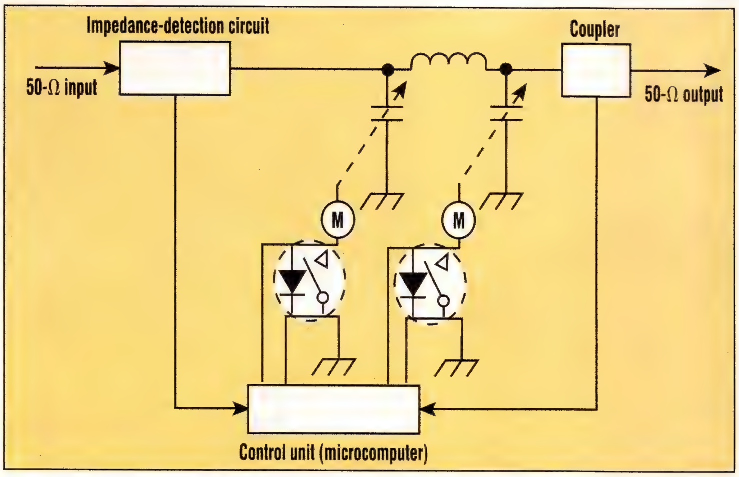

5. Unlike transistor switches, LED-MOS relays work quite well in parallel, helping solve some involved application problems.

[redacted]

time analysis as possible. This would require readings of each process variable every few microseconds, instead of the millisecond intervals obtainable with conventional reed relays. The system used 16 inputs and the process cycle allowed 10 ms to analyze data coming from all 16 inputs as well as produce and display results. The data was read sequentially and the analysis results were displayed. The reed relays that sampled these inputs were quite fast for an electromechanical relay—1 to 2 ms. Both analog and digital signals were involved.

To gain the required speed for real-time analysis, conventional SSRs were first tried. While considerably faster than the reeds, they struggled trying to handle analog signals. At this point, the designers learned about LED-MOS relays, whose output FETs switch even low-level analog signals quite well. Units designed for low-signal switching with turn-on times between 0.1 to 0.3 ms were selected, and the available analysis time was increased over 10 times.

Yet another LED-MOS-specific application involved an aircraft-control system that experienced problems with EMRs used to switch 400-Hz currents supplying certain lamp loads. Lamp loads are notorious for their high in-rush currents—a typical lamp load can draw up to 10 times its steady-state current at a cold turn-on. Because the switching could not be timed to occur at the zero crossover, contacts would burn out regularly.

A solution involving conventional SSRs failed, because the zero crossover problem still remained. Finally the answer came in using the power LED-MOS relays, which could handle up to 4 A of current and avoid zero-crossover problems.

Another general LED-MOS capability that helps solve telecommunication problems is their ability to work in parallel, which is almost impossible for conventional transistor switches. This permits them to be used in automatic tuning control circuits that work with communication-satellite receiving equipment *(Fig. 5)*.

Douglas J. Lionetti, marketing manager for Aromat Corp., holds a BSEE and an MS in business administration from Stevens Institute of Technology, Hoboken, N.J.

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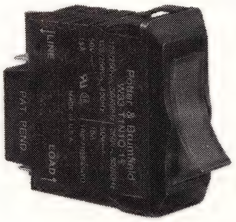
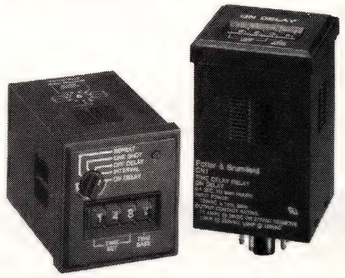


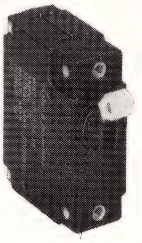
One- or two-pole sensing, two-pole breaking model offers current ratings from 5 through 20A. W33 provides circuit protection, on/off switching and an optional indicator lamp in a single, compact package. Snaps into panel cutout without tools. Designed to meet international standards.

CN1/CNM5 Time Delay Relays



Low-cost units time from 0.1 sec. to 9,990 hrs. with digital accuracy. CN1 is an on-delay timer. CNM5 provides five different timing functions. Each model is housed in a 1/16 DIN enclosures and has a DPDT output relay rated 10A @ 240VAC. 8-pin (CN1) or 11-pin (CNM5) plug-in base.

W6 Magnetic Circuit Breaker



VDE APPROVED MODELS NOW AVAILABLE

Breaker is offered in one- through four-pole models for current ratings from 200mA through 50A. Recent line extensions include snap-mount models and types with single actuators for multiple poles. Series offers various trip-time delays, circuit functions, mountings and actuator options.

Potter & Brumfield
A Siemens Company

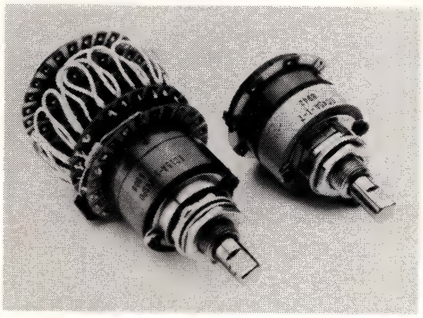
9401

READER SERVICE 101

SWITCHES & RELAYS

▼ ROTARY SELECTORS MOUNT ON PC BOARDS

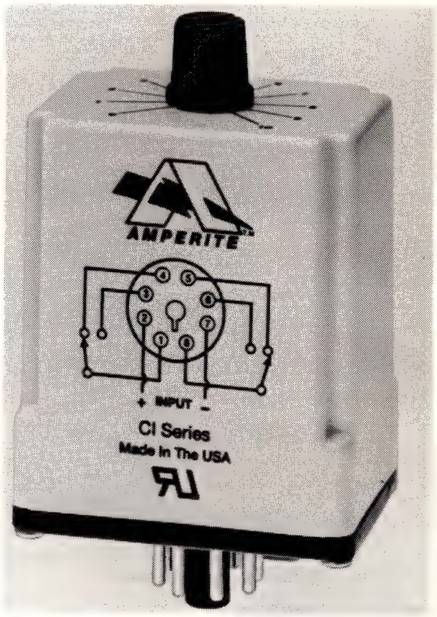
Totally enclosed, explosion-proof, and unitized construction is featured in the Series E printed-circuit rotary selector switches. The switches perform more complex functions than standard decimal-output rotary types. Their maximum current capacity is 0.125 A. Special coded outputs are housed in miniature and microminiature bodies to accommodate high-density specifications. These small switches encompass independent coded outputs and additional circuitry coupled with potentiometers and integral resistors. Call for pricing and delivery.



Janco Corp.
3111 Winona Ave.
Burbank, CA 91504
(818) 846-1800
▶CIRCLE 700

▼ TIME-DELAY RELAY NEEDS NO ACTIVATOR

There's no need for an activating switch with the CI Series time-delay relay. Upon application of input power, the relay's contacts will transfer for the specified interval. Features include interval-on circuitry with durable relay contacts. The double-pole, double-throw unit switches up to 10 A with repeatability of ±5% and timing tolerance of ±5%. Timing can be fixed or adjustable by means of a top-mounted knob. List price is $39.25 with quantity discounts available. Small quantities are delivered from stock.



Amperite Co. Inc.
600 Palisade Ave.
Union City, NJ 07087
(800) 752-2329
▶CIRCLE 701

SWITCH & RELAY MANUFACTURERS

AMP Inc.
P.O. Box 3608
Harrisburg, PA 17105-3608
(800) 522-6752
(DP) (PC) (PS) (PG)
(RO) (SL) (SM)
CIRCLE 800

AT&T Microelectronics
555 Union Blvd.
Dept. 500404200
Allentown, PA 18103
(800) 372-2447
(AS) (DS) (HF) (OI) (TE)
CIRCLE 801

Advanced Components Industries
Gruner Div.
1308 Sartori Ave. #105
Torrance, CA 90501
(310) 328-0060
(FP) (ML) (PB) (PW)
CIRCLE 802

American Control Technology
1447 Holmes Rd.
Elgin, IL 60123-1203
(708) 468-6000
(PC) (PG) (TH)
CIRCLE 803

American Zettler Inc.
75 Columbia St.
Aliso Viejo, CA 92656
(714) 831-5000
(AS) (FP) (HS) (PB) (PW) (TE)
CIRCLE 804

Amperite Co. Inc.
600 Palisade Ave.
Union City, NJ 07087
(201) 864-9503
(TD)
CIRCLE 805

Aromat Corp.
Automation Controls Div.
629 Central Ave.
New Providence, NJ 07974
(908) 464-3550
(LI) (PC) (PH) (PX) (SA) (SM)
(TS) (AS) (AU) (CT) (DS)
(DR) (FP) (HD) (HF) (IO) (ML)
(OI) (PB) (PW) (TE) (TD)
CIRCLE 806

Arcolectric Corp.
9001 Canoga Ave.
Canoga Park, CA 91304
(818) 700-1933
(IL) (PC) (PU) (RK)
(RO) (SL) (SA) (TG)
CIRCLE 807

Bourns Inc.
1200 Columbia Ave.
Riverside, CA 92507
(909) 781-2517
(PU) (RO) (SM)
CIRCLE 808

Brentek International Inc.
150 W. Beaver St.
York, PA 17406
(717) 755-8000
(DR) (HD) (HS) (IO)
(OI) (PW) (TD) (VS)
CIRCLE 809

Burgess-SAIA Inc.
Switch Div.
1335 Barclay Blvd.
Buffalo Grove, IL 60089-4527
(708) 215-9600
(KL) (PC) (PH) (PX)
(PU) (SA) (SM)
CIRCLE 810

C & K Components Inc.
Clayton/Unimax Div.
8182 U.S. 70 West
Clayton, NC 27520-9058
(800) 334-7729
(IL) (KL) (MR) (PC) (PU)
(RK) (RO) (SL) (SA)
CIRCLE 811

C & K Components Inc.
Newton Div.
15 Riverdale Ave.
Newton, MA 02158
(800) 635-5736
(DP) (IL) (KB) (MR) (MB)
(PC) (PS) (PX) (PU) (RK)
(RO) (SL) (SM) (TH) (TG)
CIRCLE 812

CP Clare Corp.
Dyad Products Div.
48 Progress Pkwy.
Maryland Heights, MO 63043
(314) 434-0311
(MR) (PC) (SM) (AS) (AU)
(CS) (DS) (DR) (FP) (HS)
(IO) (ML) (MW) (MI) (PB)
CIRCLE 813

CP Clare Corp.
Solid State Products Div.
107 Audubon Rd., 8 Corp. Pl.
Wakefield, MA 01880
(617) 246-4000
(AS) (CS) (DS) (OI)
CIRCLE 814

CTS Corp.
Electrocomponents Div.
1142 W. Beardsley Ave.
Elkhart, IN 46514
(219) 295-3575
(DP) (RK) (RO) (SL)
CIRCLE 815

Cambridge Aeroflo Inc.
900 Mt. Laurel Circle
Shirley, MA 01464
(508) 425-2346
(AP)
CIRCLE 816

Carroll Touch
P.O. Box 1309
Round Rock, TX 78680
(512) 388-5615
(TS)
CIRCLE 817

Cole Instrument Corp.
2650 S. Croddy Way
Santa Ana, CA 92704
(714) 556-3100
(AC) (KL) (PC) (PG)
(RO) (SA) (ST) (SM)
CIRCLE 818

Communications Insts. Inc.
CII Midtex Div.
9B2 Butterfield Trail
El Paso, TX 79906
(915) 772-1061
(AS) (CX) (HD) (HS)
(ML) (MW) (PB) (PW)
(TE) (TD) (VS)
CIRCLE 819

Connect-Tech Products
1472 W. Long Ave.
Littleton, CO 80120
(800) 967-5224
(LI) (PC) (PU) (RK) (SL)
(SA) (SM) (TG)
CIRCLE 820

Contaq Technologies Corp.
15 Main St.
Bristol, VT 05443
(802) 453-3332
(PS) (PG) (PX)
CIRCLE 821

Control Components & Systems
557 Long Rd.
Pittsburgh, PA 15235
(412) 371-1111
(AS) (AU) (DS) (DR) (HS)
(IO) (MW) (MI) (PB)
CIRCLE 822

Coto Wabash
55 Dupont Dr.
Providence, RI 02907-3105
(401) 943-2686
(MR) (PX) (SM) (AS) (CX)
(CS) (DS) (DR) (HS) (HF)
(ML) (MW) (PB) (TE) (VS)
CIRCLE 823

Crouzet Corp.
3237 Commander Dr.
Carrollton, TX 75006
(800) 677-5311
(KL) (LI) (PC) (PH) (PX) (PU)
(RK) (SA) (TH) (AS) (CS)
(DS) (DR) (PB) (TD) (VS)
CIRCLE 824

Crydom Co.
6015 Obispo Ave.
Long Beach, CA 90805
(310) 865-3536
(AS) (DS) (HD) (OI)
(PB) (PW) (TD)
CIRCLE 825

Deltrol Controls
Deltrol Corp.
2745 S. 19th St.
Milwaukee, WI 53215
(414) 671-6800
(PW)
CIRCLE 826

(see p. 134 for key)
(continued on p. 130)

High-end rack for high-end tech.

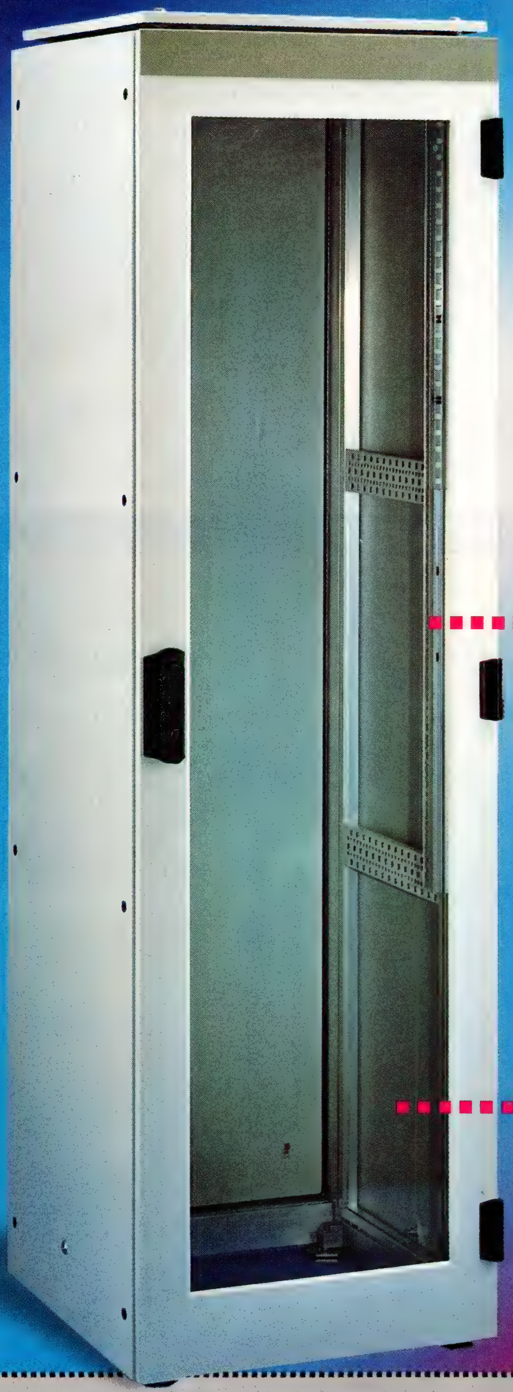
Come what may: miracel is the rack system with space for 19" and metric components. miracel sets other standards for enclosures – new mounting nuts, self-aligning components, and favourable balance between weight and stability facilitate transportation and assembly. Another feature – doors with 180° opening angle and door reversal opening on left or right.

Altogether a real advance.

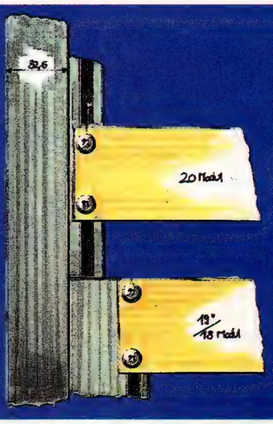
READER SERVICE 90

miracel®

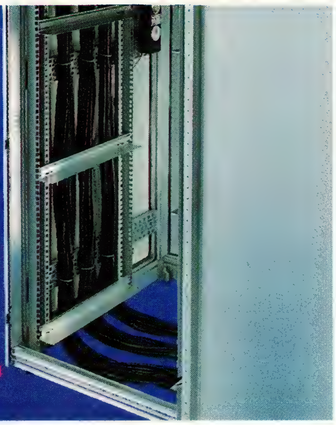
multiuse industrial rack for electronics



Future-proof: Every component fits – 19" or metric. That cuts out future reorganization costs.



miracel feature: 82% of the overall space available as installation space. Even in racks 600 mm wide there is space at the sides.



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I am interested in miracel:

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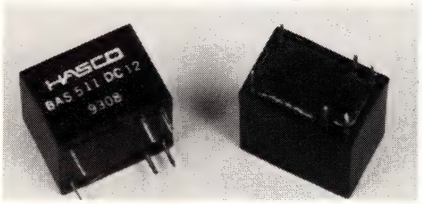
▼ MINIATURE 5-A RELAY MEETS TELECOM SPECS

By increasing its current-handling capacity, Hasco has expanded its miniature BAS Series relays into 1-, 2-, and 5-A capacities at 60 V dc/120 V ac. Dimensions are 0.44 in. tall by 0.62 in. long by 0.43 in. wide. All relays in the series meet FCC Part 68 telecommunication specifications and are fully sealed. Dc-coil voltages range from 3 V to 48 V. Pricing is $0.59 in lots of 10,000. Delivery of small quantities is from stock.



Hasco Components Int'l Corp.
247-40 Jericho Tpke.
Bellerose Village, NY 11001
(516) 328-9292
▶ **CIRCLE 702**

▼ QUICK-MOUNT SSRs LATCH ELECTRONICALLY

Lower installed costs for the OEM assembler result from using the NIF Series of quick-mounting solid-state relays. Screw terminals are replaced by 1/4-in. quick connects. The latching relays provide a flip-flop function. Each time a control voltage is applied, the output changes state and latches. The control voltage is optically isolated from the output (operating) voltage. Operating voltages of 24, 120, or 230 V ac (50/60 Hz) and input-coil voltages of 9 to 290 V ac/dc are standard. The electronically latching triac output can be either normally open or closed. Rating is 6, 10, or 20 A steady with zero-voltage or random-on switching. Call for pricing and delivery.

SSAC Inc.
P.O. Box 1000
Baldwinsville, NY 13027
(315) 638-1300
▶ **CIRCLE 703**

▼ TINY PUSHBUTTONS SHRUG OFF STATIC

The possibility of faulty actuations caused by operator-induced buildups of static electricity is eliminated in the Series B super-subminiature pc-board pushbutton switches. An anti-static carbon-impregnated bushing is used with a metal support bracket that routes static charges from the operator directly to the board. Instead of passing through the contacts, these stray charges are shunted to ground. In addition, the units are totally sealed to prevent contact contamination during processing. Momentary and alternate actions are available in SPDT or DPDT configurations. All switches are rated at 0.4 VA maximum at 28 V ac/dc maximum. Call for pricing and delivery.

NKK Switches
7850 E. Gelding Dr.
Scottsdale, AZ 85260
(602) 991-0942
▶ **CIRCLE 704**

SWITCH & RELAY MANUFACTURERS

Dialight Corp.
1913 Atlantic Ave.
Manasquan, NJ 08736
(908) 223-9400
(IL) (PU)
CIRCLE 827

EAO Switch Corp.
198 Pepe's Farm Rd.
Milford, CT 06460
(203) 877-4577
(IL) (KL) (LI) (MB) (PC) (PU)
CIRCLE 828

Electro-Mech Components Inc.
1826 Floradale Ave.
El Monte, CA 91733-3689
(818) 442-7180
(IL) (PU)
CIRCLE 829

Electromatic Controls Corp.
A Carlo Gavazzi Group Co.
2495 Pembroke Ave.
Hoffman Estates, IL 60195
(708) 882-5757
(PH) (PX) (AS) (CS)
(DS) (DF) (FP) (HS)
(PB) (PW) (TD) (VS)
CIRCLE 830

Elma Electronic Inc.
44350 S. Grimmer Blvd.
Fremont, CA 94538-6385
(510) 656-3400
(DP) (IL) (KB) (KL) (LI) (MB)
(PC) (PU) (RO) (SM) (TG)
CIRCLE 831

Euchner-USA Inc.
300 Roundhill Dr., Unit 4
Rockaway, NJ 07866
(201) 586-2600
(MR) (PH) (PX) (PU) (RO)
(SA)
CIRCLE 832

Farnell Components
18 Technology Dr.
Irvine, CA 92715
(714) 727-3001
(KB) (AS) (DS) (FP) (HF)
(ML) (PB) (PW) (VS)
CIRCLE 833

Fujitsu Microelectronics
Electronic Components Div.
3545 N. First St.
San Jose, CA 95134-1804
(800) 642-7616
(AU) (DR) (FP) (HD) (HS)
(ML) (PB) (PW) (TE) (VS)
CIRCLE 834

GEM Electronics Inc.
160 Fernwood Dr.
East Greenwich, RI 02818
(401) 885-8454
(CS) (DR) (HF) (MW) (PB)
(PW) (TE) (VS)
CIRCLE 835

Gentron Corp.
7345 E. Acoma Dr.
Scottsdale, AZ 85260
(602) 443-1288
(AS) (CS) (DS) (HS) (MI) (PW)
CIRCLE 836

GlobTek Inc.
186 Veteran's Dr.
Northvale, NJ 07647
(201) 784-1000
(IL) (PC) (PU) (RK) (RO) (SL)
(SA) (TH) (TG) (AS) (DS)
CIRCLE 837

Gordon Engineering
67 Del Mar Dr.
Brookfield, CT 06804
(203) 775-4501
(PX)
CIRCLE 838

Grayhill Inc.
561 Hillgrove Ave.
P.O. Box 10373
La Grange, IL 60525
(708) 482-2132
(DP) (KB) (KL) (PC)
(PU) (RO) (SM) (AS) (DS)
(IO) (OI) (PB) (PW)
CIRCLE 839

Hallmark Technologies Inc.
1717 E. Lincoln Ave.
Mt. Dora, FL 32757
(904) 383-8142
(KB) (MB) (SA)
CIRCLE 840

Hasco Components Int'l. Corp.
247-40 Jericho Tpke.
Floral Park, NY 11001
(516) 328-9292
(MR) (AU) (DR) (FP) (HD)
(HS) (PB) (PW) (TE)
CIRCLE 841

Haydon Switch & Instrument Inc.
1500 Meriden Rd.
Waterbury, CT 06705
(203) 756-7441
(LI) (PU) (RK) (SA) (TG)
CIRCLE 842

Hermetic Switch Inc.
P.O. Box 1325
3100 Hwy. 92 S.
Chickasha, OK 73023
(405) 224-4046
(LI) (PX) (DR)
CIRCLE 843

Honeywell
Micro Switch
11 W. Spring St.
Freeport, IL 61032
(800) 537-6945
(AP) (IL) (KB) (KL) (LI) (MR)
(PC) (PH) (PS) (PX) (PU) (RK)
(RO) (SA) (SM) (TG)
CIRCLE 844

ITW Switches
6615 W. Irving Park Rd.
Chicago, IL 60634
(312) 282-4040
(IL) (LI) (PC) (PU) (RK)
(RO) (SL) (SA) (SM)
CIRCLE 845

IVO Industries Inc.
34 Industrial Way East
Eatontown, NJ 07724
(908) 542-5151
(PH) (PX)
CIRCLE 846

Inresco Inc.
2411 Atlantic Ave.
Manasquan, NJ 08736
(908) 223-6330
(MB) (PX) (DR) (MW)
CIRCLE 847

International Rectifier
Advanced Products Dept.
233 Kansas St.
El Segundo, CA 90245
(310) 607-8862
(AS) (DS) (OI) (PB) (TE)
CIRCLE 848

Janco Corp.
3111 Winona Ave.
Burbank, CA 91504-0038
(818) 846-1800
(IL) (KL) (PC) (PG) (PU) (RO)
CIRCLE 849

Joslyn Jennings Corp.
Jennings Div.
970 McLaughlin Ave.
San Jose, CA 95122
(408) 292-0358
(CO) (CX) (CT) (CS)
(HF) (MI) (PW)
CIRCLE 850

Kilovac Corp.
P.O. Box 4422
Santa Barbara, CA 93140
(805) 684-4560
(AU) (CT) (HD) (HS) (HF) (IO)
(ML) (MI) (PB) (PW)
CIRCLE 851

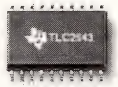
Lamb Industries Inc.
4826 S.W. Scholls Ferry Rd.
Portland, OR 97225
(503) 297-8878
(AP) (DP) (IL) (KB)
(PC) (PU) (RK) (RO)
(SL) (SA) (SM) (TG)
CIRCLE 852

Littelfuse Inc.
800 E. Northwest Hwy.
Des Plaines, IL 60016
(708) 824-1188
(PU) (AU)
CIRCLE 853

(see p. 134 for key)
(continued on p. 132)

What's the brightest news in A/D price and performance in 1994?

TI's new TLC2543 12-bit A/D converter at a 10-bit price.



The TLC2543 from Texas Instruments sets a new price/performance point in the marketplace. Its power dissipation is only 5 mW typical. That's 50 percent lower than most 12-bit A/D converters, at about half the cost.

The right stuff. With the TLC2543 you get an on-board 14-channel multiplexer that offers 11 analog-input channels and three self-test channels. This 12-bit A/D converter has a 10-µs maximum conversion time and sample and hold. Plus a system clock and 8-bit control register. And an end of conversion flag makes it easy to interface with microprocessors and DSPs.

TLC2543 Features

- 12-bit resolution A/D converter
- 10-µs maximum conversion time
- Low power consumption — 5 mW (typ), 13 mW (max)
- Power-down mode — 125 µW
- Standard serial interface
- On-chip system clock
- 11 analog-input channels
- Available in 20-pin SOIC, DIP or PLCC packages

New Members of TI's A/D Family

Device	Supply Voltage	Input/ Output	Conversion Speed (Max)	Resolution
TLC2543	5.0 V	11 ch/serial	10 µs	12 bits
TLV1549	3.3 V	1 ch/serial	21 µs	10 bits
TLC1549	5.0 V	1 ch/serial	21 µs	10 bits
TLV1543	3.3 V	11 ch/serial	21 µs	10 bits
TLC1541/43	5.0 V	11 ch/serial	21 µs	10 bits
TLC1550	5.0 V	1 ch/parallel	6 µs	10 bits
TLC1225	5.0 V	1 ch/parallel	12 µs	12 + sign

The TLC2543 in 3.3-V and shrink small-outline versions is on the horizon.

Where you need it. Use the TLC2543 in automotive, instrumentation and a broad range of industrial applications, including motor control, robotics, numerically controlled machine tools and data logging.

Easy migration. Its pinout is compatible with the TLC543 8-bit and TLC1543 10-bit A/D converters from TI. So upgrades are easily achieved with only minor software adjustments.

Convert today. Get 12-bit A/D performance at a 10-bit price. To find out how easy it is, call your local TI office, return the reply card by mail or fax it to **886-2-377-1460.**

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TEXAS INSTRUMENTS

Australia & New Zealand: Sydney, 61-2-878-9000, fax 61-2-805-1186; Melbourne, 61-3-696-1211, fax 61-3-696-4446. **Hong Kong:** 852-737-0338, fax 852-735-4954. **Korea:** 82-2-551-2800, fax 82-2-551-2828.
Malaysia: 60-3-230-6001, fax 60-3-230-6605. **People's Republic of China:** 86-1-500-2255, ext. 3750, fax 86-1-500-2705. **Philippines:** 63-2-817-6031, fax 63-2-817-6096.
Singapore (& India, Indonesia, Thailand): 65-350-8100, fax 65-253-6655. **Taiwan:** 886-2-713-9311, fax 886-2-716-9487.

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SWITCH & RELAY MANUFACTURERS

MGR Industries Inc.
450 B Industrial Dr.
Fort Collins, CO 80524
(303) 221-2201
(IL) (KB) (MB) (PU)
CIRCLE 854

MORS/ASC
P.O. Box 544
Wakefield, MA 01880
(617) 246-1007
(DP) (IL) (KL) (PC) (PG) (PU)
(RK) (RO) (SL) (SA) (SM)
(TH) (TG) (TS) (PB)
CIRCLE 855

Mantex Corp.
Electronics Div.
P.O. Box 15
Oxford, MI 48371
(810) 628-8210
(MB) (PC)
CIRCLE 856

Marquardt Switches Inc.
2711 Route 20E
Cazenovia, NY 13035
(315) 655-8050
(KB) (PU) (RK) (SL)
(SA) (TG)
CIRCLE 857

Matrix Systems Corp.
5177 N. Douglas Fir Rd.
Calabasas, CA 91302
(818) 222-2301
(CX) (DR) (HS) (MW) (TE)
CIRCLE 858

McGill Electric Switch Group
1002 N. Campbell St.
Valparaiso, IN 46383
(219) 465-2379
(PU) (RK) (SA) (TG)
CIRCLE 859

Micropac Industries Inc.
Solid State Relays Div.
P.O. Box 469017
Garland, TX 75046
(214) 272-3571
(AS) (DS) (MI) (OI) (PW)
CIRCLE 860

Molex Inc.
Switch Products Div.
2222 Wellington Ct.
Lisle, IL 60532
(708) 969-4550
(MB) (PU)
CIRCLE 861

NKK Switches
7850 E. Gelding Dr.
Scottsdale, AZ 85260
(602) 991-0942
(DP) (IL) (KL) (PC) (PU) (RK)
(RO) (SL) (SM) (TG)
CIRCLE 862

NTE Electronics Inc.
44 Farrand St.
Bloomfield, NJ 07003
(201) 748-5089
(AS) (AU) (DS) (DR) (FP)
(IO) (PB) (PW) (TD)
CIRCLE 863

Norstat Inc.
300 Roundhill Dr., Unit 4
Rockaway, NJ 07866
(201) 586-2500
(AS) (CS) (IO) (TD) (VS)
CIRCLE 864

OakGrigsby Inc.
88 N. Dugan Rd.
Sugar Grove, IL 60554-0890
(708) 556-4200
(IL) (KL) (PC) (PG) (PU) (RO)
CIRCLE 865

Omega Engineering Inc.
One Omega Dr.
Stamford, CT 06907
(203) 359-1660
(AC) (AP) (LI) (MR) (PC)
(PG) (PX) (RO) (CT) (CS)
(DS) (DF) (DR) (IO) (ML)
(MW) (RT) (VS)
CIRCLE 866

Omron Electronics Inc.
One E. Commerce Dr.
Schaumburg, IL 60173
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Costa Mesa, CA 92627
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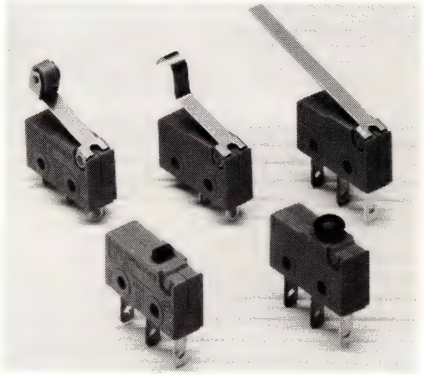
(see p. 134 for key)

(continued on p. 134)

▼ SNAP-ACTION SWITCH OFFERS VERSATILITY

A variety of interchangeable actuators, with or without rollers, can be used with the 1050 Series snap-action switches. One option is a mushroom-shaped actuator that works at any angle up to 45°. Life expectancy for the devices is over 1 million cycles.



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2711 Route 20 East
Cazenovia, NY 13035
(315) 655-8050
▶ CIRCLE 705

▼ TIME-DELAY RELAYS OFFER HIGH ACCURACY

Two highly accurate, low-cost time-delay relays have been added to P&B's line. The CNM5 is a five-function programmable device, while the CN1 provides the most commonly used timing function, delay-on-operate. Both are housed in 1/16-DIN enclosures with round plug-in bases for socket mounting. The CNM5 has an 11-pin base, while the CN1 has an 8-pin base. Each provides a microprocessor-based timing circuit controlling a DPDT electromechanical-relay output. The CNM5 model's functions include on delay, off delay, interval, recycle with equal on- and off-time, and one-shot. Pricing is $52 for the CNM5 and $42 for the CN1.

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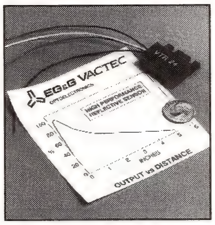
(812) 386-2559
▶ CIRCLE 706

▼ LONG RANGE SENSING IN MATCHBOX SIZE



Ideal for applications requiring object sensing and material control. The VTR24F1 retro-reflective optical switch extends the range of contactless, optical position sensing. Almost the size of a matchbox, it senses objects up to 4 inches. Designed to "see" almost any surface including matte, gloss, or black, this sensor provides a switchlike response, low position error, and CMOS compatibility.

EG&G Optoelectronics
Vactec Division
10900 Page, St. Louis, MO 63132
Phone (314) 423-4900
Fax: (314) 423-3956

READER SERVICE 194

▼ IR EMITTER AND DETECTOR CHIPS

Choose from an extensive line of photodiodes, photodiode arrays, phototransistors and IRED chips for OEM assembly applications. Photodiodes and photodiode arrays are available in both solderable and wire bondable configurations. Custom services are also offered.

The IREDs are manufactured in 880 nm (GaAlAs) and 940 nm (GaAs) peak emission wavelengths using a state-of-the-art liquid phase epitaxial process which produces high power output and long operating lifetimes with a minimum of degradation.

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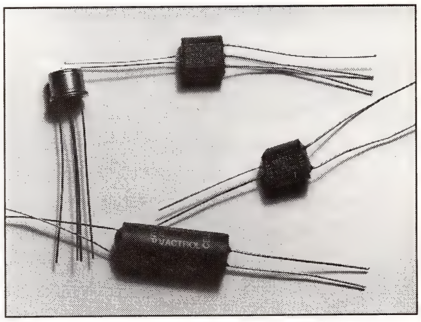
READER SERVICE 195

▼ IDEAL FOR AUDIO APPLICATIONS

Analog Optoisolators (Vactrols™) are ideal as power limiters and remote gain control in audio amplifiers. Used widely in professional and automobile audio equipment, Vactrols™ provide low noise and low harmonic distortion making them ideal for use as electronically adjusted variable resistors. The Vactrols™ catalog discusses audio applications such as gating, muting, limiters, AGC distortion, and switching.



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Vactec Division
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Phone (314) 423-4900
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READER SERVICE 196

▼ OPTIMIZED OPTICS

The VTE1285 high output IR Emitting Diode (IRED) incorporates an aspheric lens to optimize the amount of power focused into its output beam. This 5 mm diameter plastic package contains a 880 nm high efficiency IRED chip. Typical power output at 100 mA drive is 20 mW. Typical total half power beam angle is 16 degrees. A companion part, the VTE1295 is U.L. Component recognized. Applications include smoke detectors, remote controls, and security systems.

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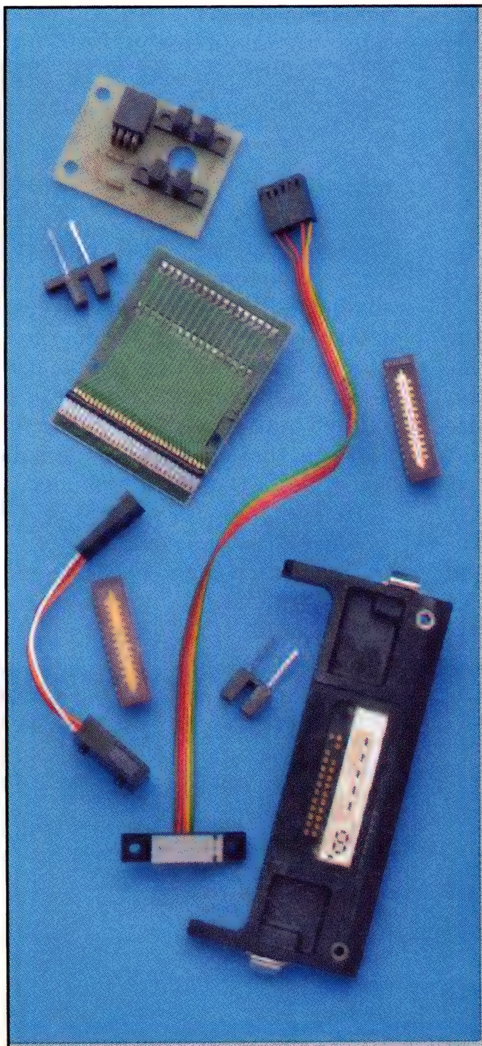

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▼ DC-COIL RELAYS HANDLE HIGH CURRENTS

Current handling up to 30 A is available in the AZ 2100 Series of low-cost dc-coil relays. The devices come in several different popular footprints, have complete UL and CSA approvals, feature pc or quick-connect terminals, and are offered in Form A, B, and C contact configurations. Class B insulation (130°C) is standard, and relays can be ordered with Class F insulation (155°C) for higher-temperature applications. Other available types include general-purpose relays as well as units that switch from dry circuits to high currents. Call for pricing and delivery.

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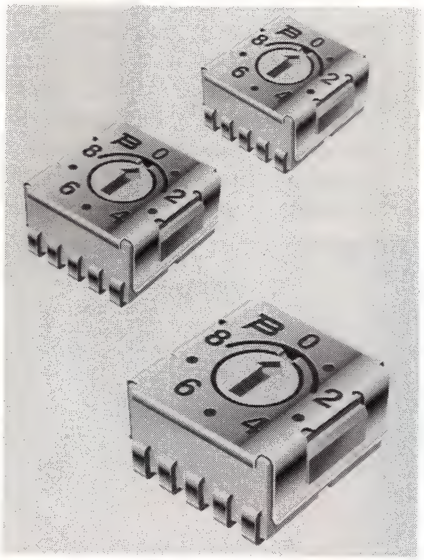
▼ MINI SELECTOR SWITCHES HELP WITH DOWNSIZING

The 7600 Series of sealed, ultra-miniature selector switches are single-pole, multiple-throw styles with detent-type top actuators. The 6-mm model 7643 (shown) has nine throws and one "off" position. The 4-mm model 7644 has four throws and one "off" position. Both are intended for designers who want to downsize their end products without sacrificing performance. Initial contact resistance is specified at 100 mΩ maximum. Operation is from –55 to 125°C. Pricing in lots of 1000 is $1.14 and $1.53 for surface-mount versions of the 7644 and 7643, respectively. Through-hole prices are slightly higher.



Bourns Inc.
1200 Columbia Ave.
Riverside, CA 92507
(909) 781-5500
▶CIRCLE 708

▼ I/O OUTPUT MODULES EASE CONTROL DESIGNS

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Teledyne Inc.
Solid State Div.
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Hawthorne, CA 90250
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Los Angeles, CA 90066
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(ML) (OI) (DS) (TD)
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Hawthorne, CA 90250
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(HS) (HF) (ML) (MI) (PB)
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Membrane Switch Div.
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CIRCLE 890

Tricon Industries Inc.
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Reach Electronic Inc.
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Lexington, NE 68850
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(IL) (KB) (MR) (PC) (PU) (SM)
CIRCLE 892

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CIRCLE 893

Xymos Technologies Inc.
8225 W. Parkland Ct.
Milwaukee, WI 53202
(800) 869-9669
(KB) (MB)
CIRCLE 894

KEY

Switches

(AC)	Acceleration
(AP)	Air-pressure
(CO)	Coaxial
(DP)	DIP
(IL)	Illuminated
(KB)	Keyboard
(KL)	Keylock
(LI)	Limit
(MR)	Magnetic reed
(MB)	Membrane
(PC)	Pc-mounted
(PH)	Photoelectric
(PS)	Piezoelectric
(PG)	Programmable
(PX)	Proximity
(PU)	Pushbutton
(RK)	Rocker
(RO)	Rotary
(SL)	Slide
(SA)	Snap-action
(ST)	Stepping
(SM)	Surface-mounted
(TH)	Thumbwheel
(TG)	Toggle
(TS)	Touch screens

Relays

(AS)	Ac solid-state
(AU)	Automotive
(CX)	Coaxial
(CT)	Contactors
(CC)	Crystal-case
(CS)	Current-sensing
(DS)	Dc solid-state
(DF)	Differential
(DR)	Dry reed
(FP)	Flat-pack
(HD)	Heavy-duty
(HS)	Hermetically sealed
(HF)	High-frequency
(IO)	Input/output
(ML)	Magnetic latching
(MW)	Mercury-wetted reed
(MI)	Military/aerospace
(OI)	Optical isolation
(PB)	Pc-board
(PW)	Power
(RT)	Rotary
(TE)	Telephone
(TD)	Time-delay
(VS)	Voltage-sensing

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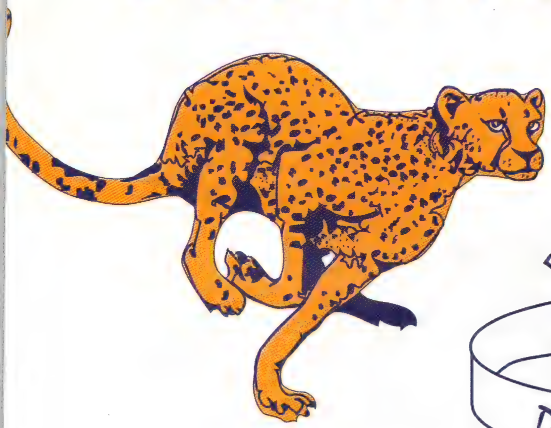

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READER SERVICE 83

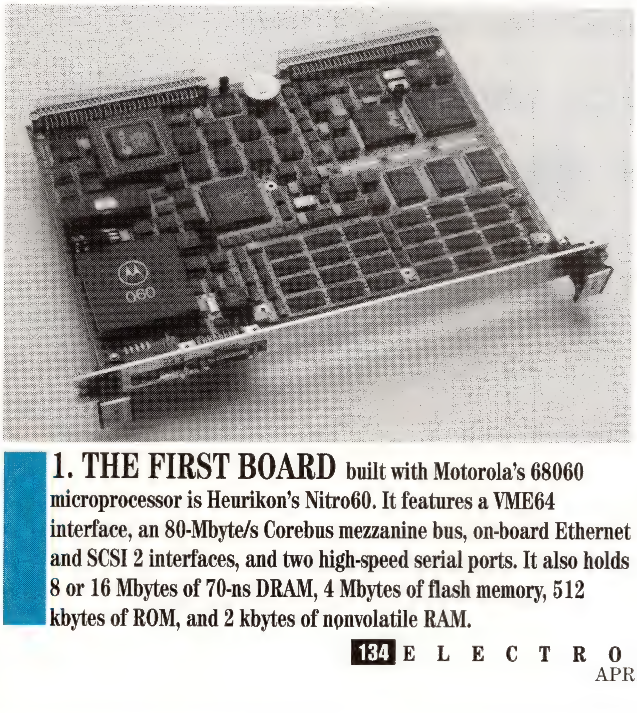
68060 CPU FORMS THE HEART OF VMEBUS BOARD

AS THE 68060 ROLLS OFF THE PRODUCTION LINE, THE NITRO60 CPU BOARD WILL BE NIPPING AT ITS HEELS.

RICHARD NASS

When new microprocessors are released, they're usually followed by announcements of the system boards that house them. The release of Motorola's 68060 microprocessor certainly is no exception to that trend. In fact, the first of what will be many upcoming board announcements comes from Heurikon Corp. The company's Nitro60 board, which offers an upgrade path for systems powered by earlier-generation 68040-based boards, is built to the VMEbus specification.

The Nitro60 features an optimized VME64 system-bus interface, an 80-Mbyte/s Corebus mezzanine (local-bus) interface, on-board Ethernet and SCSI 2 interfaces with direct memory access, and two high-speed serial ports. It also holds 8 or 16 Mbytes of 70-ns DRAM, 4 Mbytes of flash memory for application storage, 512 kbytes of ROM, and 2 kbytes of nonvolatile RAM *(Fig. 1)*. The nonvolatile RAM holds such user-definable parameters as default baud rates, software and hardware revision levels, and system configuration information. The majority of the flash memory, 3.5 Mbytes, is user accessible. The remaining 512 kbytes are reserved for monitor and power-diagnostic utilities.



1. THE FIRST BOARD built with Motorola's 68060 microprocessor is Heurikon's Nitro60. It features a VME64 interface, an 80-Mbyte/s Corebus mezzanine bus, on-board Ethernet and SCSI 2 interfaces, and two high-speed serial ports. It also holds 8 or 16 Mbytes of 70-ns DRAM, 4 Mbytes of flash memory, 512 kbytes of ROM, and 2 kbytes of nonvolatile RAM.

When Heurikon's designers developed the Nitro60 board, they didn't actually have a CPU to work with (the 68060 processor is being sampled now). To get around this problem, a 68040 chip was substituted for much of the design, because the two processors are fairly compatible. Since all register addresses are the same, the code from the 68040 board was ported directly to the 68060 version. In addition, the map—the component layout—of the two boards is almost identical, including the VME and peripheral addresses.

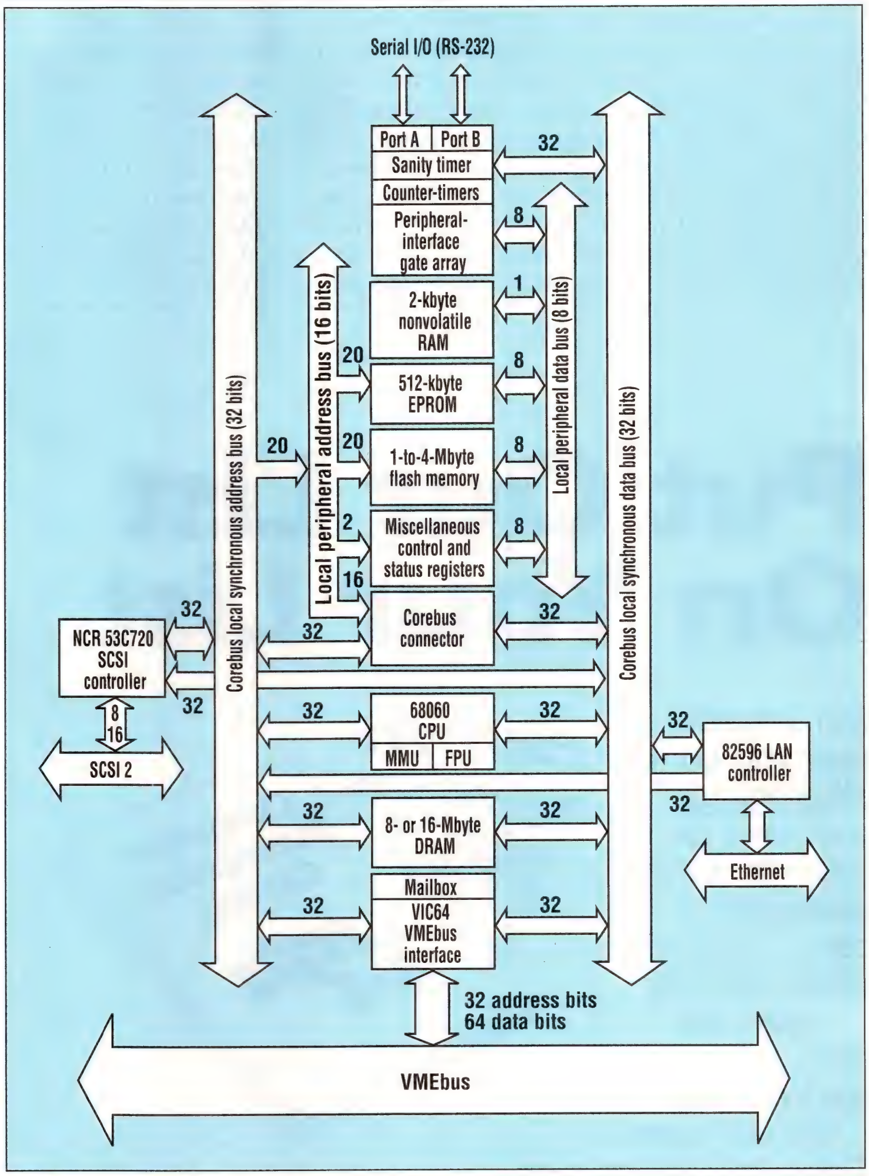
When nearing the end of the design process, the engineers discovered that they had developed about 90% of a complete 68040-based board, whose performance level was just a shade below that of the Nitro60. Hence, the company decided to release the Nitro40, which is nearly identical to the Nitro60, except it contains the previous-generation microprocessor, the 68040.

The Nitro60 is aimed at graphics-oriented applications that require high-speed I/O and data transfers, such as printing, image processing, and simulation. It's also suited for data-acquisition, embedded-control, and communication applications, which often require high-speed buffer manipulation.

The 68060 processor chip is built with a clock-doubling technique—a popular addition in the latest generation of microprocessors. It runs at an internal clock rate of 50 MHz. Its external speed, the speed that the rest of the board runs at, is 25 MHz. With a peak performance of 100 MIPS, the 68060 is fully compatible with the 68040, employing a superscalar architecture with dual four-stage pipelines. It also contains an 8-kbyte instruction cache, an 8-kbyte data cache, and a 256-entry branch cache. In addition, the 68060 is 100%-compatible with the 68040 instruction set.

To speed memory accesses, the Nitro60's DRAM employs a two-way bank-interleaved architecture with write-posting buffers. It also can handle page-mode transfers. This architecture enables the main-memory subsystem to support burst-mode write operations with no wait states. Burst-mode read operations incur three wait states for the first read, none for the second, one for the third, and none for the fourth. Transparent discrete hardware refreshing is also supported with one parity bit per byte. The 512 kbytes of ROM can be configured in increments of 64, 128, or 512 kbytes.

Data-movement and I/O operations are expedited by the DMA-intensive architecture that encompasses the high-speed system bus, as well as the Ethernet, serial, and mezzanine-bus interfaces *(Fig. 2)*. The VME64 interface, which is based on the standard Cypress VIC64 VME interface chip, employs FIFO buffers to decouple the local bus and VMEbus. As a result, both buses can run simultaneously at their maximum speeds.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Port A
Port B
Sanity timer
Counter-timers
Peripheral-interface gate array
2-kbyte nonvolatile RAM
512-kbyte EPROM
1-to-4-Mbyte flash memory
Miscellaneous control and status registers
Corebus connector
68060 CPU
MMU
FPU
8- or 16-Mbyte DRAM
Mailbox
VIC64 VMEbus interface
NCR 53C720 SCSI controller
SCSI 2
82596 LAN controller
Ethernet
Corebus local synchronous address bus (32 bits)
Local peripheral address bus (16 bits)
Local peripheral data bus (8 bits)
Corebus local synchronous data bus (32 bits)
32 address bits
64 data bits
VMEbus
32
8
1
20
2
16
8
16

2. THE DMA-INTENSIVE ARCHITECTURE of the Nitro60 board encompasses the system bus; Corebus; and Ethernet, serial, and SCSI 2 interfaces. The VME64 interface, which can operate in a master or slave mode, employs FIFO buffers to decouple the local bus and VMEbus.

The VME64 interface, which can operate in a master or slave mode, supports four-level arbitration and seven VMEbus interrupts, as well as mailbox interrupts that allow the board to be controlled remotely through VMEbus-specified addresses. This feature makes possible such functions as CPU reset, interrupt, and VMEbus lock. The local DMA capability can handle 32- or 64-bit block transfers.

The board's Ethernet interface is based on Intel's 32-bit 82596CA local-area-network (LAN) coprocessor. Supporting Ethernet data-transfer rates up to 10 Mbits/s, the 82596CA's FIFOs and integrated DMA controller buffer the data while increasing the data-transfer rate between the Ethernet LAN and the Nitro60's local memory bus.

An NCR 53C720 chip forms the basis of the ANSI-compatible fast and wide SCSI 2 interface. The interface features a synchronous data-transfer rate of 20 Mbytes/s and an asynchronous rate of 10 Mbytes/s. It's built with a 32-bit DMA controller to perform memory-to-I/O data transfers without requiring any host intervention. The board supports 32-bit-word data bursts with variable-size burst lengths. Other features of the interface include support for up to seven independent I/O controllers and both variable block size and scatter-gather data transfers. Through the P2 connector, the board can accept 8-bit single-ended or 16-bit differential connections.

Two front-panel serial ports can pass data at a rate up to 1 Mbit/s, depending on cable length. Each port supports both asynchronous and synchronous transfers, using Intel 8251A universal asynchronous receiver-transmitter (UART) emulation. Each port also includes an internal baud-rate generator that's completely controlled by software. In addition, the front panel houses a reset-interrupt switch and a seven-segment LED display. A built-in real-time clock offers a 10-ms resolution, while three 32-bit counter-timers each have 62.5-ns resolution.

ADDING FLEXIBILITY

Thanks to the built-in Corebus mezzanine interface, designers and users can customize the Nitro60. Consequently, various options for upgrading the memory, the processor, and the I/O ports are available using a series of modules offered by Heurikon. Because Corebus is an open specification, designers are free to develop their own daughtercards to suit a specific application. In addition, Heurikon offers a series of modules, including most standard I/O types. The Nitro60's 32-bit Corebus interface runs at 25 MHz (one-half the 68060's internal speed) and supplies a peak performance of 80 Mbytes/s.

The Nitro60 VMEbus board fits an industry-standard 6U form factor (9.19 by 6.3 in.). It operates in the 0° to 55°C temperature range.

Software support for the Nitro60 includes two real-time operating systems: VxWorks developed by Wind River Systems Inc., Alameda, Calif.; and OS-9 from Microware Systems Corp., Des Moines, Iowa. Heurikon maintains and supports both operating systems in-house. Hence, the company can tailor those operating systems to suit a specific customer's application, including solving complex integration problems. Heurikon is also a source-code licensee for VxWorks. ☐

PRICE AND AVAILABILITY

With 8 Mbytes of DRAM, the Nitro60 VMEbus single-board computer sells for $5495. In the same configuration, the Nitro40, with its 33-MHz 68040 CPU, is priced at $4995. The Nitro40 is sampling now and will go into production in June. The Nitro60 will go into production as soon as Motorola releases large quantities of the 68060 microprocessor.

Heurikon Corp., 8310 Excelsior Dr., Madison, WI 53717; (800) 356-9602 or (608) 831-0900. **CIRCLE 511**

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PRODUCTS NEWSLETTER

DIGITAL-VIDEO ENCODER TRIMS MULTIMEDIA COST

Supporting both composite and higher-fidelity Y/C video outputs without external buffers and other costly circuits, the Bt851 digital video encoder chip from Brooktree Corp., San Diego, Calif., lets designer build low-cost consumer products such as interactive multi-player, and set-top decoders. Included on the chip are circuits that handle RGB and YCrCb color spaces (so the Bt851 can support popular game applications in the RGB color space), as well as a voltage reference and four on-chip video DACs. Outputs on the chip include dual Y and C signals to deliver high-quality S-video signals, and a pair of composite-video outputs, so both baseband video and composite outputs to drive channels 3 and/or 4 are simultaneously available. The Bt851 features are highly configurable, allowing designers to implement a system that uses either DIP switches or external logic to configure the encoder's features. Housed in a 68-lead PLCC, the digital video encoder sells for less than $10 each in large volumes. Samples are available now. For more information, contact Brooktree at (619) 452-7580. *DB* **CIRCLE 930**

CORE LOGIC EASES 486, PENTIUM-BASED DESIGNS

A single-chip core logic solution for "green" 486-class motherboards, a PCI bridge chip, and a green buffer chip—all developed by OPTi Inc., Santa Clara, Calif.—help reduce system complexity and ease the design of 486- and Pentium-based computers. The 82C802G single-chip core-logic circuit is aimed at power-conserving green 486-class logic boards and supports Level-1 write-back caches, system-management interrupts, and stop-clock mode. The chip also includes two power-saving modes: auto-green and SMI-green. The first works autonomously; the latter is controlled through the SMI features on the CPU. In addition, the chip also controls up to eight DRAM banks, includes Level-2 write-back cache support, and provides a VESA VL-bus interface. The 82C602 green buffer chip provides a real-time clock and all of the bus interface buffers; the 82C822 provides a VL-bus-to-PCI bridge for systems that need the added flexibility of PCI compatibility. For Pentium-processor support, the company also offers the 82C596 and 82C597, a two-chip set that implements all of the main system-board logic, including a full 64-bit cache bus that runs at 60 or 66 MHz. Samples of all chips are available now. In lots of 10,000 units, the 82C802G sells for $12 each; the 82C822 goes for $15; the 82C602 costs $4; and a set consisting of the 82C596, 597, and the 82C206 I/O chip costs $65/set. Call OPTi at (408) 980-8178. *DB* **CIRCLE 931**

INEXPENSIVE 486SX RUNS AT 50 MHZ

A clock-doubled 486SX that runs at 50 MHz internally provides designers with a new performance/price point for entry-level systems. The Am486SX2-50, from Advanced Micro Devices, Austin, Texas, includes the Am486 CPU core with an 8-kbyte internal write-through cache. It comes in a DX2-compatible, 168-lead PGA that can drop into sockets already in place for the DX CPUs. The 50-MHz CPU gives system users who don't need the floating-point performance of the DX-class parts the same integer performance of the 486DX2-50. In lots of 1000 units, the 486SX2-50 sells for $165 each. Contact AMD at (512) 385-8542. *DB* **CIRCLE 932**

DRIVE CONTROLLERS UP BUFFER BANDWIDTH

High-end hard-disk drives will profit from the AIC-8300 family of disk controllers. The ICs offer a 16-bit, 40-Mbyte/s buffer bandwidth. Both hardware and software error correction is implemented. In addition, a byte-wide three-way Reed-Solomon error-correction code adds to the performance improvement. Other features include automated data-flow management and automatic read and write cache support. The family builds on the previous-generation AIC-8200 family of controllers. The 8370 operates through the Fast IDE interface, modes 3 and 4. It's also compatible with ATA modes 0 through 2. The 8320, for SCSI-based drives, is designed with a fully programmable RAM sequencer. An evaluation board is available, as well as a series of programming and development tools. Samples of either chip cost $20. The 8370 is sampling now, with production beginning in the late summer or fall. The 8320 will sample in June, with production starting three to six months later. *RN* **CIRCLE 933**

Edited by Clifford Meth

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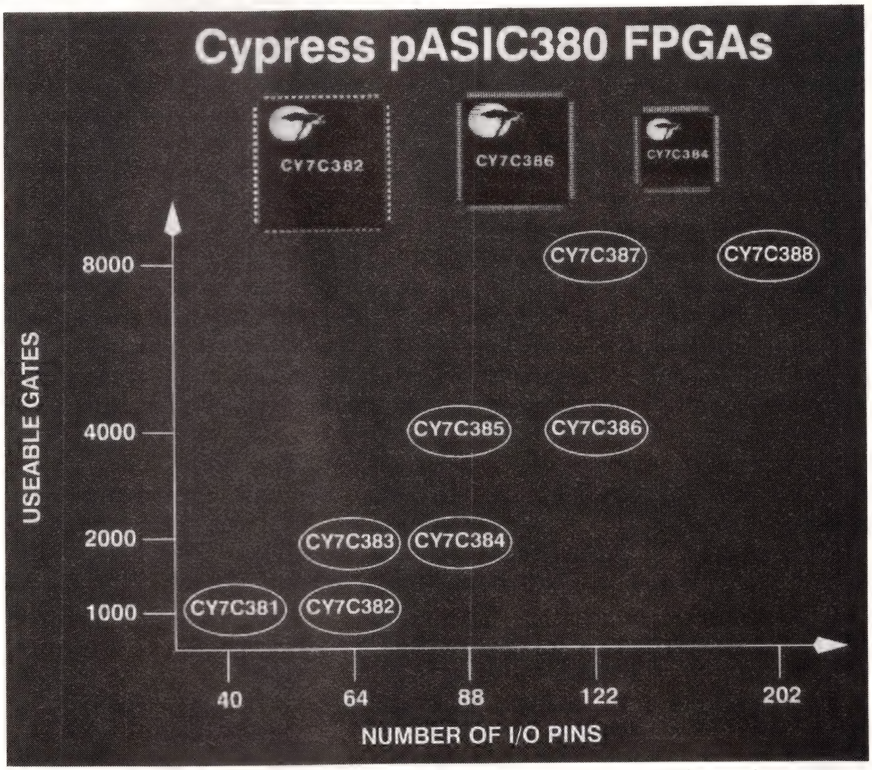
ENHANCED FPGA FAMILY TRIMS DELAYS, UPS GATE COUNT AND FLEXIBILITY

DAVE BURSKY



Shrinking the gate dimensions by about 35% to just 0.65 µm—versus the 1-µm features used in the first-generation QuickLogic FPGA—designers at Cypress Semiconductor created a second-generation family with shorter delays, higher gate capacities, and better usability. These FPGAs offer up to 8000 usable gates. Loadable counters based on these FPGAs can operate at over 100 MHz, with chip-to-chip operating speeds of up to 85 MHz, and a basic input-to-output delay from one pin, through one logic cell, and out another pin of less than 9 ns.

Based on an enhanced version of the QuickLogic ViaLink one-time programmable antifuse configuration element, the pASIC family delivers about 50% better performance than chips in the previous family. The smaller features and improved antifuse cell shrink the programming elements to one-third the size of cells used in competing antifuse-based solutions; less than one-eighth the size of an SRAM-based configuration cell. The smaller elements also allow more routing resources on the surface of the chip. As a result, the company's Warp 3 design tools allow the automatic-placement-and-routing software to 100% place and route all designs. The pASIC380 series—a second-generation version of the FPGA family licensed from QuickLogic—starts with 1000-usable-gate (3000-available-gate) chips, the CY7C381 and 382, and ups the complexity to 2000 usable gates for the CY7C383 and 384, to 4000 on the CY7C385 and 386, and to a top of 8000 gates on the CY7C387 and 388. The pairs of chips with the same density differ in the number of I/O cells—32 and 56 for the 1000-gate FPGAs, 56 and 68 for the 2000-gate units, 68 and 114 for the 4000-gate chips, and 114 and 194 cells, respectively, for the 8000-gate FPGAs. In total, the number of I/O pins, including dedicated inputs, ranges from 40 to 202 pins.

The very regular architecture of the resulting chips also provides highly predictable timing delays, which in turn minimizes the affect that small design changes have on circuit performance. Each chip starts with an array of logic cells, each of which contains a pair of six-input AND gates, four two-input AND gates, three 2:1 mulitplexers, and a D flip-flop, which can be configured as a J-K, S-R, or T-type. Each cell represents about 30 gate equivalents of logic capacity and offers features that represent the best of coarse-grain and fine-grain cell structures. Each cell also has five outputs, and the logic can be separated into smaller "fragments"—one flip-flop, and two independent six-input AND gates. The cell can implement all possible Boolean transfer functions with up to three variables, plus many with up to 14 variables.

The logic cell also includes separate Set and Reset inputs that can asynchronously control the output state of the flip-flop. Consequently, the combination of wide gating and the built-in register with asynchronous set and reset, makes the cell an ideal building block for high-speed state machines, shift registers, encoders, decoders, arbitration, and arithmetic logic. Because of the simple structure and small fuse area, more antifuses can be employed to give the arrays a very high level of flexibility. They contain more than four times as many programmable elements as in SRAM-based FPGAs. Designs are also highly testable, with a built-in scan path that permits factory testing of the logic and the I/O cells. The Warp 3 design tools include automatic test-vector-generation support to test devices after programming. They also include waveform simulation with back-annotation of net delays after placement to the design net list.

Samples of the CY7C381 through 386 are available; samples of the CY7C387 and 388 are expected in the third quarter. In 100-unit lots, the 84-lead PLCC 4000-gate CY7C385 costs $95.50. In large quantities, the 1000-gate CY7C381 will sell for under $10 by the second half of 1994.

Cypress Semiconductor Corp., 3901 N. First Street, San Jose, CA 95134; (408) 943-2600. **CIRCLE 620**

CRYPTO ENGINE EASES PUBLIC-KEY SECURITY

At the heart of a family of portable public-key security products, a custom-designed 32-bit microcontroller with an embedded cryptography engine provides designers with a tamper-proof approach to implement portable tokens. These "tokens," which are based on the first open, published standard for public-key cryptography (PKCS 11), can be implemented in formats as small as type-1 cards defined by the Personal Computer Memory Card Industry Association (PCMCIA). The iPower security processing unit (SPU) can consequently be embedded in PCMCIA-format cards and carried by personnel to control access to critical data, or to identify a user.

Developed by National Semiconductor, the iPower secure microcontroller holds the encryption algorithms, secret data, and the central processing unit that processes them. The chip was designed to remain secure from electrical probes through the signal pins, as well as from analytical probes that etch away the package and circuit layers. Any such penetration would cause the stored data to be "zeroed" before it could be read out. The iPower SPU consists of a 32-bit CPU core with on-chip ROM, a real-time clock, and a interface to off-chip nonvolatile (battery-backed) RAM that holds scrambled data. The remaining blocks on the chip include the encryption engine, some battery-backed RAM to hold secured data (master keys, algorithms, or records), and a host-system bus interface. The SPU chip can be combined with off-chip low-power RAM, a battery, and a PCMCIA interface to squeeze the entire public-key token on a card that meets the PCMCIA's type-1 format.

The cards, dubbed Tessera after the token ancient Romans used as a ticket or means of identification, can now be implemented at a relatively low cost (less than $100 per user for large orders) compared with previous solutions. Nevertheless, it provides the highest level of commercial security (FIPS 140-1, level 3). Encrypted data could provide positive identification of users, store private medical records, include authorization codes, or even perform secure transaction processing.

National Semiconductor Corp., *2900 Semiconductor Drive, M/S 16-225, P.O. Box 58090, Santa Clara, CA 95052-8090; Walt Curtis, (408) 721-8797.* **CIRCLE 621**

■ *DAVE BURSKY*

SINGLE-CHIP COMBINES CACHE CONTROLLER AND MEMORY SUBSYSTEM

Taking advantage of its memory-based ASIC technology, Sony Components Products has created a single-chip cache controller/memory subsystem for 80846-based computer systems. The CXK784862Q combines all the cache control logic, 160 kbits of tag memory, and 256 kbytes of cache memory on a single chip to form a two-way, set-associative 256-kbyte second-level cache.

Housed in a 160-lead PQFP, the cache subsystem operates at system clock rates of 33 or 50 MHz, and provides the smallest area level-two cache for 80486-based desktop and portable computers.

The cache operates in a look-aside mode and makes it possible for designers to implement true zero-wait-state systems with 2-1-1-1 burst timing. Employing a write-through cache protocol, the cache memory is organized as 32 kwords by 36 bits (including parity) by two banks, and uses a 16-byte line size. The accompanying tag random-access memory (RAM) is organized as 4 kwords by 20 bits by two banks.

Designed to work with most motherboard logic chip sets, the CXK784862Q was already tested with motherboard logic chips, such as LSI Logic's HT340 and PicoPower's PT86C268.

Multiple chips can be cascaded to create caches of up to 1 Mbyte. This capability was made possible without any glue logic, thanks to a proprietary interface dubbed "enhanced cascading mode," which Sony engineers developed.

When powered by a 5-V supply, the CXK784862Q cache-controller/memory chip consumes less than 2 W, when run at 50 MHz. That power level is considerably lower than the power consumed by a multichip cache design.

Samples of the controller/memory are immediately available and in lots of 100 units sell for $125 apiece. In lots of 5000 units, the chip's price drops to $100 each.

Sony Components Products Company, *10833 Valley View Street, P.O. Box 6016, Cypress, CA 90630-0016; Jack Koplic, (714) 229-4189.* **CIRCLE 622**

■ *DAVE BURSKY*

GRAPHICS ACCELERATOR COMBINES FUNCTIONS

The TGUI9420DGi, a three-in-one accelerator, integrates a graphics accelerator, a clock synthesizer, and a d- converter. The DRAM-based board combines a 32-bit frame-buffer interface, a fixed-function graphics engine, a 24-bit true-color DAC, and an 80-MHz dual clock synthesizer. The high level of integration reduces design complexity by decreasing the overall component count. This results in a simplified motherboard implementation or add-in board design. Graphics performance receives a boost through hardware acceleration of frequently used operations, including BitBLTs, line drawing, rectangle fills, text transfer, color expansion, and hardware-cursor support. A command FIFO buffer helps balance the computing load and data flow without degrading CPU performance. Designs can be based on the ISA bus, or the PCI or VL-Bus local buses. The chip fits in a 208-pin plastic quad flat pack. In lots of 1000, the TGUI9420DGi costs $21 each. RN

Trident Microsystems Inc., 205 Ravendale Dr., Mountain View, CA 94043; (415) 691-9211.

CIRCLE 623

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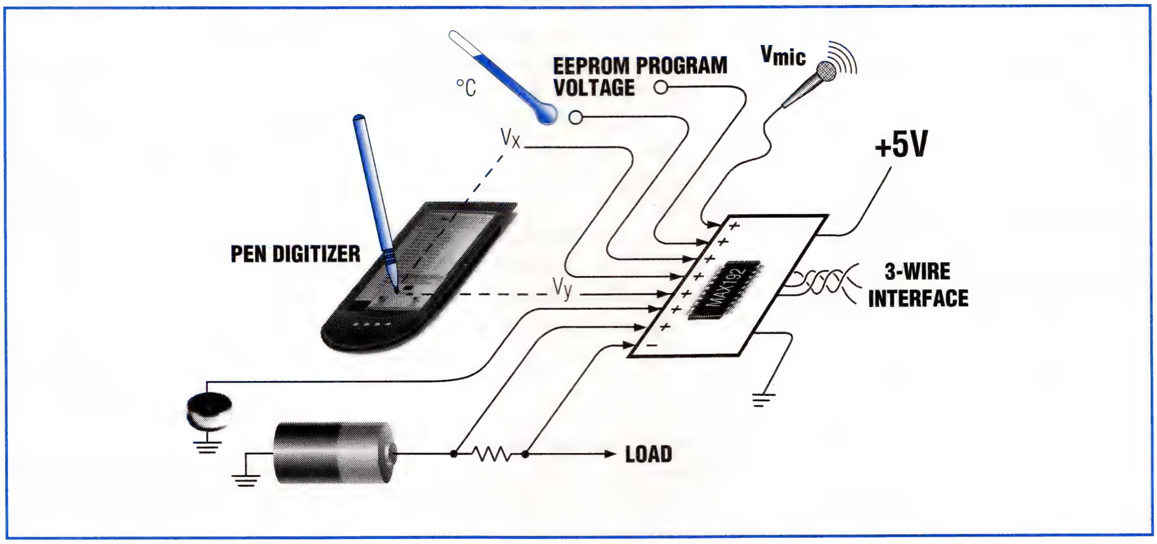

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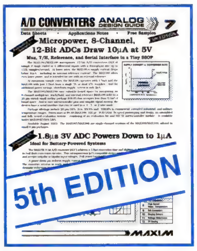
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READER SERVICE 145

SPARC-BASED NOTEBOOK COMPUTER SERVES AS DESKTOP REPLACEMENT

With the third generation of a Sparc-based notebook computer, users can now get almost all of the features of a desktop workstation. The Sparcbook 3 is built with a 50-MHz microSparc processor. Weighing about 7 lbs. (nearly 10 lbs. when fully configured with external battery and charger), the platform contains two Type 2 PCMCIA slots, which can hold two Type 1 or 2 cards, or one Type 3 card; a color TFT display; a 1-Mbyte frame buffer; and an 8-bit audio capability. While system memory ranges from 16 to 64 Mbytes using SIMMs, data is retained by a removable 2.5-in. hard-disk drive. Two options are available—340 or 520 Mbytes. The system can also be configured with a monochrome passive display.

The Sparcbook 3 comes preloaded with SunSoft's Solaris 1 or 2 operating environment, and Version 2.0 of Tadpole's Nomadic Computing Environment, a user-friendly graphical interface and power-management system that supports mobile Unix computing.

The system's magnesium case is designed for portability, as well as ruggedness. When used as a desktop replacement, it can connect to a Sun-compatible keyboard, an external display, and a mouse. Built-in ISDN capability permits remote networking, telephony, or teleconferencing applications. Also, running SunSoft's WABI (Windows Application Binary Interface) or SoftWindows, from Insignia Solutions, the Sparcbook 3 can run any PC-compatible software. Additional external connections can be made through on-board Ethernet, SCSI 2, parallel or serial ports.

A fully loaded Sparcbook 3 sells for $10,950. The monochrome version, called the Sparcbook 3LC, costs $7500. Peripherals, such as removable disk drives and various PCMCIA devices, are also available from the company.

***Tadpole Technology Inc.**, 12012 Technology Blvd., Austin, TX 78727; (512) 219-2200.* **CIRCLE 624**

■ *RICHARD NASS*

TWO-HEAD PARALLEL DRIVE CUTS TRANSFER RATE IN HALF

Although two-head parallel disk drives have sold for about a year, until recently, they only found their way into high-end drives employing Intelligent Peripheral Interfaces (IPIs). Now these drives are available with a SCSI interface on the Barracuda 2 3.5-in. form-factor drive.

Traditionally, users requiring the high data rate afforded by the two-head parallel technique were involved with high-end (as opposed to mainstream) applications. Now, it's not uncommon to see 1-Gbyte disk drives on the desktop—a mainstream interface is warranted to reduce the cost and to appeal to a larger body of users. Hence, two-head parallel drives now come with SCSI interfaces. Another reason the drive lacked a SCSI interface was that there were no supporting electronics. But Seagate designed its own components to support the dual-head approach with a SCSI interface.

The two-head parallel disk drive reads and writes from two heads at the same time to double the data rate. Typically in a drive, a request is issued, and the actuator is moved and then used to read data from the selected head. Using the two-head parallel approach, some of the electronics are duplicated. So there are two read chains, or two sets of electronics that read and write to the disk. The heads are grouped in pairs, so when the command is issued to read data, the data is read from two heads at the same time, but not from the same platter. The drive has the built-in intelligence to select the pair of heads that's most appropriate. The data comes from two heads, halving the time required to read the data.

The two data streams are combined on a bit basis within the electronics. At the interface, the two-head parallel appears to the system as a standard drive, but with twice the transfer rate—currently about 68 to 114 Mbits/s, depending on the application.

The Barracuda 2 drive is available now in a fast and wide SCSI-2 configuration, with a 1.78-Gbyte capacity. Its average read and write seek times are 8 and 9 ms, respectively. With a 1-Mbyte cache, it costs $1800. Samples are available now and production should commence in the second quarter.

***Seagate Technology Corp.**, 920 Disc Dr., Scotts Valley, CA 95066; (408) 438-6550.* **CIRCLE 625**

■ *RICHARD NASS*

DOUBLE-SPEED CD-ROM DRIVE GOES MOBILE

The multipurpose Reno Personal CD-ROM Player is a high-performance, double-speed external CD-ROM drive that can be powered from either NiCd batteries or from an ac source. As a result, it can operate with either portable or stationary computers.

The drive connects to the PC through a SCSI port. Consisting of the drive and a docking connector, the Reno can transfer 306 kbytes/s, with an access time of under 180 ms, due to a 64-kbyte buffer. A complete multimedia kit is available. Several popular interactive CD-ROMs are bundled with the drive. Available now, the Reno CD-ROM drive ranges from $300 to $549, depending on configuration. RN

Media Vision Inc., 47300 Bayside Pkwy., Fremont, CA 94538; (510) 770-8600. **CIRCLE 626**

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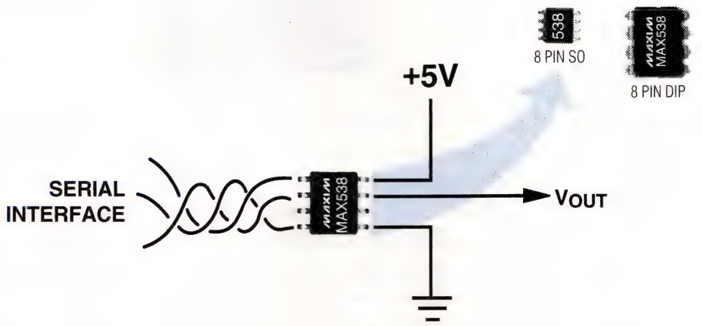

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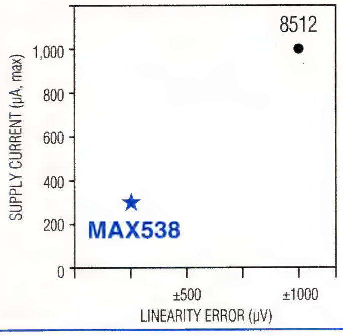

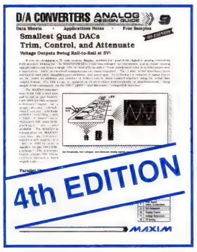
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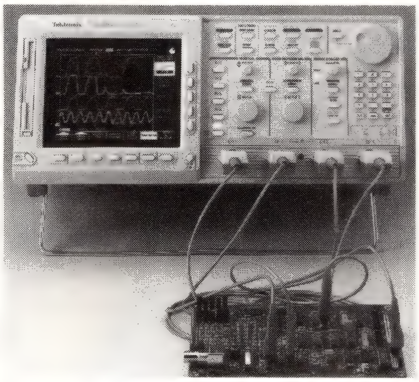
READER SERVICE 147

1-GHZ, 5-GSAMPLES/S DSO AIMS AT DIGITAL CIRCUIT DEBUG



With a bandwidth of 1 GHz and a sample rate of 5 Gsamples/s on all four channels, the TDS684A digital real-time oscilloscope specifically targets performance verification and debug of fast digital circuits. The scope's 15,000-point record length allows it to capture up to 3 μs of data at the fastest sweep speed.

The instrument offers 25 automatic measurements, with time measurements to better than 50 ps. Using the proprietary Tristar digital signal processor, waveform math is performed in real-time, including live FFTs. Waveforms can be stored on a 3.5-in. DOS-format floppy disk in a number of desktop publishing formats.

An advanced trigger set includes two new trigger types—slew rate and setup-and-hold—that make it easy to find risetime and setup-and-hold violations. Ease-of-use features include the high-resolution NuColor monitor and a graphical user interface that uses more than 100 icons to make the scope's capabilities easy to learn.

An optional probe, the P6245, delivers the scope's full 1-GHz bandwidth to the probe tip. The probe's input capacitance is less than 1 pf, and it's resistance is more than 1 MΩ. In addition, a low-mass, compact structure and specialized connectors make the probe ideal for circuits employing surface-mount technology, or devices with lead widths and spacings as small as 0.50 mm (19 mil).

The TDS684A costs $29,495, with delivery in eight weeks. The P6245 probe is $1395. As an option to the TDS684A, four probes cost $5195.

Tektronix Inc., *Test and Measurement Group, P. O. Box 1520, Pittsfield, MA 01202; (800) 426-2200.* CIRCLE 627

■ *JOHN NOVELLINO*

BOARD CAPTURES SIGNALS AT 500-MSAMPLE/S RATE

The DA500 waveform capture board features a 500-Msample/s digitizing rate with 8-bit resolution. The board, which installs in ISA-bus computers, can transfer captured data at 200 Mbytes/s over the proprietary 64-bit Auxiliary Bus. An on-board memory of 256 kbytes can be expanded to 8 Mbytes with the MX5 daughter board. Eight operating modes include single-shot, segmented, and pretrigger, as well as power-down modes to minimize power dissipation. Users can select one of 27 digitizing frequencies from 312.5 kHz to 500 MHz. The included library of C-language functions was compiled in Turbo C. Complete source code is also provided. A multiplexer selects from one of two input channels, and an interleaved mode collects data from each channel alternately. The DA500 costs $6950, with quantity discounts available. Delivery is from stock to four weeks. JN

Signatec Inc., 355 N. Sheriden St., Suite 117, Corona, CA 91720; (909) 734-3001. CIRCLE 628

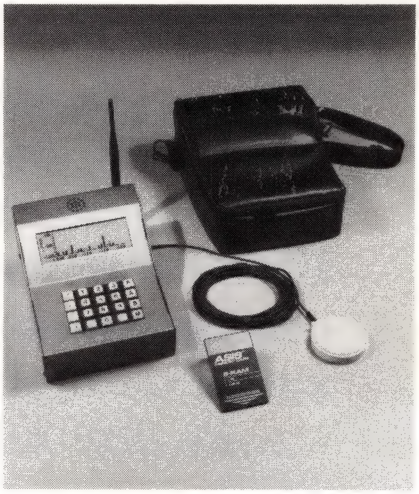
50-MHZ PORTABLE DSO USES COLOR LCD DISPLAY

With its 4-in. display, the VC-5430 subnotebook digital oscilloscope weighs less than 2 kg, battery included, and combines portability, new technology, and powerful analysis tools. Using Hitachi's High Intensity TFT Active Color LCD technology, the VC-5430's display quality approaches that of a CRT. The scope comes with 2 ksamples/channel of memory, and can digitize signals at 30 Msamples/s, with 8-bit resolution. Front-end bandwith is 50 MHz. The VC-5430 also provides for 100 internally stored waveforms. Standard features include timed data acquisition, automatic pulse parameters, and go/no-go comparison testing. In addition, the VC-5430 has both a differential input and trigger, and can be programmed via an RS-232C connector. The DSO comes with a Centronics printer interface and can support a HPGL/HP ThinkJet printer. The VC-5430 is available now for $3495. CA

Hitachi Denshi America, Ltd., 371 Van Ness Way, Suite 120, Torrance, Ca., 90501; (310) 328-6116. CIRCLE 629

SIGNAL-STRENTH METER MEASURES TO −120 DBM

A hand-held, real-time, signal-strength meter designed for RF analysis features sensitivity of −120 to −30 dBm in the 900-to-932-MHz band. A 240-by-64-pixel supertwist electroluminescent backlit LCD display presents results that mimic a spectrum analyzer in the FDM quasi-peak mode. The 3-lb. instrument works for both digital and analog modulation systems. NiCd batteries run the unit for 8 hrs. Available options include six-channel global positioning system capability and a PCMCIA memory card slot. Four other models will soon be available with overlapping coverage from 1.8 to 2.4 GHz. Custom modifications and frequencies are available on request. The meter, called the Champ, costs $1995. JN



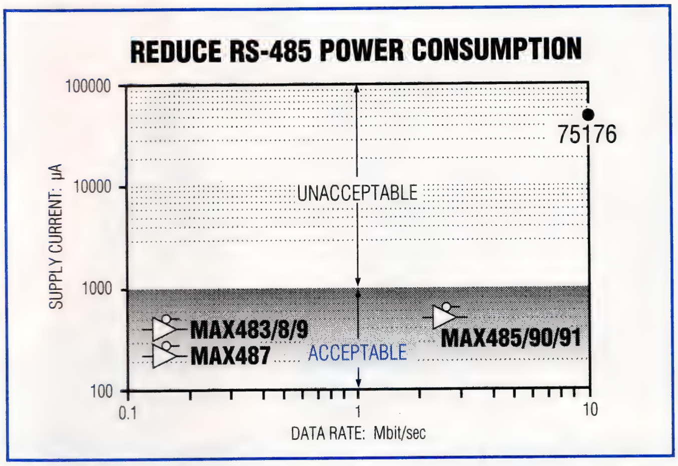
Berkeley Varitronics Systems, 255 Forrest St., Metuchen, NJ 08840; (908) 548-3737. CIRCLE 630

CUT RS-485 POWER CONSUMPTION IN HALF!

Lowest Power RS-485 IC Uses 250µA Supply Current—Max

The new MAX487 RS-485 transceiver uses a scant 250µA, making it the lowest power RS-485 IC available. The MAX487's ¼ unit load input impedance allows up to 128 transceivers on the bus at one time. Plus, slew-rate-limiting dramatically lowers radiated EMI while reducing reflections caused by mismatched cable terminations.

- **250µA Supply Current**
- **Full Duplex Available**
- **2.5Mbps Guaranteed Data Rate**
- **128 Transceivers on Bus**
- **1µA Shutdown Mode**



Specify the Optimum Low-Power RS-485 Transceiver for Your Design

	Part	#Tx/Rx	Data Rate Mbps	Max# on Bus	ISUPPLY (µA)	Full/Half Duplex	Price†	Feature
	MAX481	1/1	2.50	32	500	Half	$1.25	10µA Shutdown
	MAX483	1/1	0.15	32	350	Half	$1.25	Reduce EMI 100 Times
	MAX485	1/1	2.50	32	500	Half	$1.25	LTC485 Second Source
NEW	**MAX487**	**1/1**	**0.15**	**128**	**250**	**Half**	**$1.25**	**250µA ISUPPLY 128 MAX487s on Bus**
NEW	**MAX488**	**1/1**	**0.15**	**32**	**250**	**Full**	**$1.25**	**8-pin SO**
NEW	**MAX489**	**1/1**	**0.15**	**32**	**250**	**Full**	**$1.25**	**Separate Tx/Rx Enable**
NEW	**MAX490**	**1/1**	**2.50**	**32**	**500**	**Full**	**$1.25**	**LTC490 Second Source**
NEW	**MAX491**	**1/1**	**2.50**	**32**	**500**	**Full**	**$1.25**	**LTC491 Second Source**

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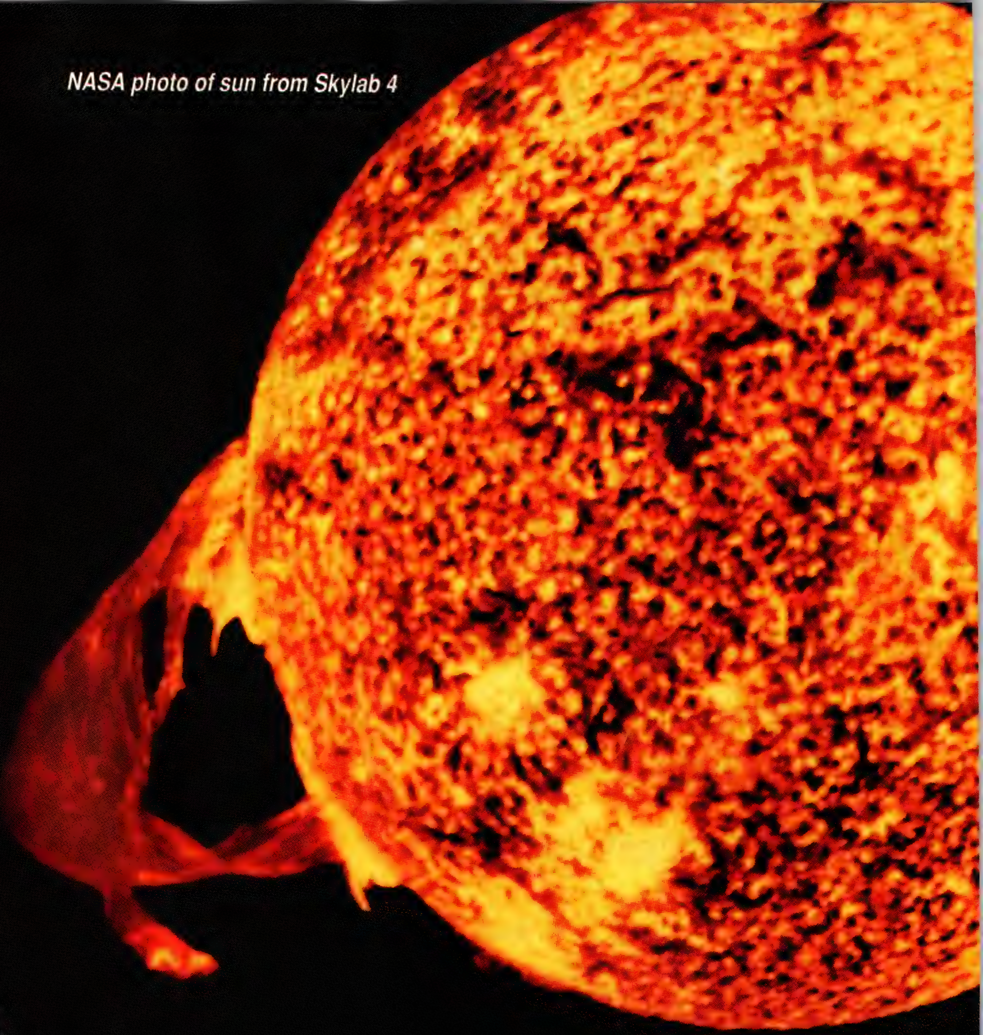
NASA photo of sun from Skylab 4



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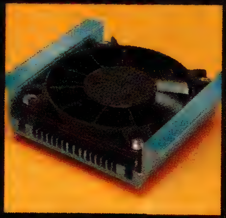

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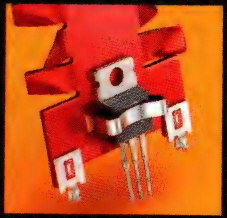

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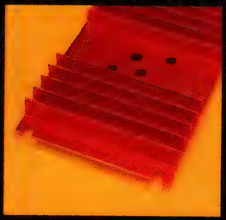
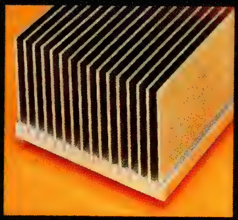


The higher the power the more we can help



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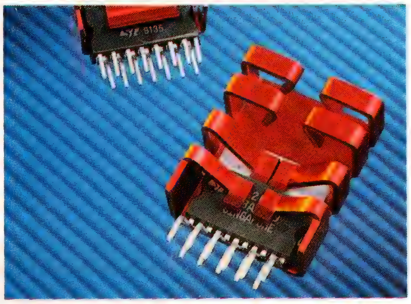

Heat sinks cool Multiwatt® ICs

Low-cost heat sinks cool Multiwatt and similar ICs. Self-locking design cuts IC assembly costs, eliminates hardware. Unique design holds ICs securely for top thermal performance. Slim and light, they take minimum board space. Low/medium power.

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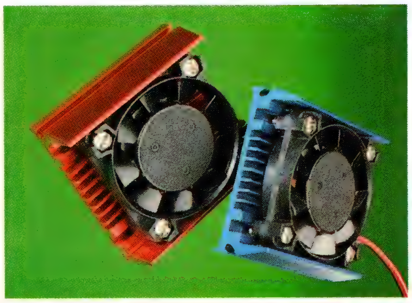

Fan/heat sinks cool Pentium™

New fan/heat sinks cool the Pentium, Alpha, Intel 80486, Motorola 68040, etc. Bidirectional, its shrouded sides maximize cooling capacity. The low profile, as little as 0.650" high, saves valuable space. Three sizes mount on 17X17, 19X19, 21X21 PGAs.

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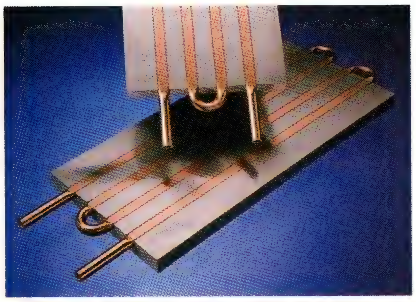

Hot concept in cold plates

New *Hi-Contact*™ liquid-cooled cold plates cool high power density electronic devices. They remove over 15% more heat, greatly reducing junction temperature. For cooling the most demanding high heat density IGBTs, other power modules.

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PRECISE RLC METERS HAVE 7-DIGIT RESOLUTION

Two RLC meters offer very high accuracy and 7-digit resolution for precise measurement of passive components and materials. The Model 7500 (±0.01%) and the Model 7400 (±0.05%) use direct digital synthesis for continuous frequency coverage from 10 Hz to 2 MHz (7500) and 500 kHz (7400). The units' large LCD screen can display parameter measurements versus test frequency, ac test voltage, or ac test current. An automated sequencing feature performs up to six independent, preprogrammed tests in series. Up to 50 test setups can be stored internally, and an optional 3.5-in. disk drive can be used to store additional setups or data in ASCII format. The Model 7500 costs $9500, and the Model 7400 costs $7500. JN

QuadTech Inc., 45 Main St., Bolton, MA 01740-1107; (508) 779-8300. **CIRCLE 631**

MOBILE TRANSMITTER TESTER WORKS VERY FAST

The MS8604A combines a 100-Hz-to-8.5-GHz spectrum analyzer and a 400-kHz-to-2.1-GHz digital-modulation analyzer into a fast, digital mobile-transmitter tester. The unit measures burst modulation accuracy in less than 1 s, and occupied bandwidth, spurious emissions, and leakage power of adjacent channels in 2 s or less. Accuracy is ±0.5 dB. Leakage power during carrier-off can be measured as an absolute value, or as an on-off ratio. The tester also makes fast measurements of frequency error, signal transmission rates, antenna power, and transmission ramp-up and ramp-down power. Measurements can be stored internally, or on a plug-in memory card. A disk drive is optional. The MS8604A costs $68,350, and delivery is in six to eight weeks. JN

Anritsu Wiltron Sales Co., 685 Jarvis Dr., Morgan Hill, CA 95037-2809; (408) 776-8300. **CIRCLE 632**

DSOS GET ADVANCED TRIGGERING OPTIONS

A set of five advanced triggering functions is now available as an option to the DataSYS 700 series digital storage oscilloscopes (DSOs). The hysteresis band triggering triggers only when the signals pass through a user-defined hysteresis band in a set direction. Band triggering triggers only when the signal enters or leaves a defined band in either direction. Runt triggering works when the signal enters or leaves the trigger band without going through both thresholds. With V-glitch triggering, the DSO triggers when the change in level between any two digitized points is more than a set amount. Finally, multichannel triggering triggers the DSO when there is a valid trigger on a selected number of input channels. The DataSYS 700 series scopes have a color display and make up to 25 automatic measurements in user-defined sequences. Display modes include Y/T, Y/degree, roll, refresh, X/Y, FFT, graphing, and histogram. The advanced triggering option (OP124) costs $650. JN

Gould Instrument Systems Inc., 8333 Rockside Rd., Valley View, OH 44125-6100; (216) 328-7000. **CIRCLE 633**

SAMPLE-HOLD CARDS CUT TIME SKEW DELAYS

The SSH-04 and SSH-08 simultaneous sample-and-hold cards help minimize or eliminate the time-skew delays that occur during analog-to-digital conversion. The cards are compatible with 12- to 14-bit conversion systems. The 8-in. long cards come with standoffs for mounting in a T-box enclosure. The units have a 1-μs sample time, an aperture uncertainty of 200 ps, and switch-selectable gains of 1, 10, 100, 200, and 500. The SSH-4 handles up to four analog inputs, and the SSH-08 eight inputs. Eight SSH-08 cards can be paralleled for 64 channels. Included are set-up, calibration, and sample programs and software drivers for popular ACCES a-d cards. The SSH-04 costs $399, and the SSH-08 costs $550. Delivery is from stock to one week. JN

ACCES I/O Products, 9400 Activity Rd., San Diego, CA 92126; (800) 326-1649. **CIRCLE 634**

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READER SERVICE 132

GRAPHICS ACCELERATORS SUPPORT 64 BITS

A new series of 64-bit PC-graphics accelerators comes in three configurations—VL-Bus, PCI, and ISA. The Kelvin 64 family increases performance using linear addressing, which offers faster access to the on-board display memory. As a result, the DRAM-based boards supply the performance of typical VRAM-based products. The Kelvin 64 complies with the VESA refresh rates and Display Power Management Standards to reduce the overall power consumption. Resolutions up to 1280 by 1024 pixels can be supported with 1 Mbyte of memory. Software drivers for most popular applications are bundled with the accelerator boards. The customized Windows driver supports zooms and pans. Available now, all three versions start at $250. RN

Orchid Technology Inc., 45365 Northport Loop West, Fremont, CA 94538; (510) 683-0300. **CIRCLE 635**

EXPANSION BOARD HOLDS 8 TRAMS

Up to eight Inmos-compatible Transputer modules (Trams) fit onto the 6U VME VME-XP expansion board. As a result, parallel-processing techniques can be used to accelerate application software development. The eight Tram sites are organized as a four-by-two mesh, with all uncommitted links routed to a hard-wired configuration area to create custom topologies. An optional compute node, the IMST805, offers 8 Mbytes of zero wait-state memory. The interface is handled through the VME P2 connector. The VME-XP sells for $595 and $2095 with the IMST805. Large-quantity discounts apply. RN

Alta Technology Corp., 9500 South 500 West, Suite 212, Sandy, UT 84070; (801) 562-1010. **CIRCLE 636**

VME SPARC ENGINE HOLDS UP TO 4 CPUS

With the ability to support up to four processors in a 6U VME form factor, the 10MP Sparc engine is 100% compatible with Sun Microsystems' SparcStation 10 family. The 10MP is built with either TI's SuperSparc or Fujitsu's hyperSparc processors. The hyperSparc ranges in speed from 55 to 80 MHz, while the SuperSparc runs from 40 to 50 MHz. The VMEbus interface supports DMA and block transfer modes in both directions. One or two MBus or SBus slots are available—if two MBus slots are used, then just one SBus slot is open, and vice versa. Other features include 32 to 256 Mbytes of DRAM, up to 1 Mbyte of cache memory, an Ethernet port, a fast SCSI 2 interface, and two serial ports. The Solaris 1.1 or 2.3 operating systems run unmodified. Real-time operating-system support includes VxWorks 5.1, VadsWorks, and RTMX. Prices start at $9995. RN

Themis Computers Inc., 6681 Owens St., Pleasanton, CA 94588; (510) 734-0870. **CIRCLE 637**

GRAPHICS BOARD FITS MACS, POWERPC SYSTEMS

The Spectrum Power 1152 is a 24-bit color graphics card that's compatible with Macintosh computers, including those built with the Power PC microprocessor. The board fits a 7-in. form factor, so it fits into the industry-standard NuBus slots. The board is suited for QuickDraw and imaging applications. As the PowerPC-based systems become available, users can upgrade their boards through downloadable software. Available now, the board sells for $1399. RN

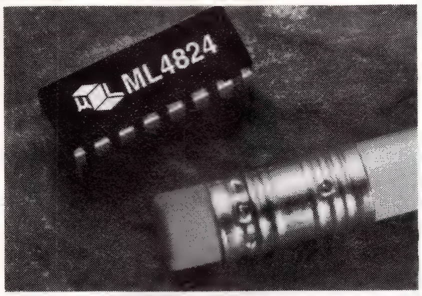
SuperMac Technology Inc., 215 Moffett Park Dr., Sunnyvale, CA 94089; (408) 541-6100. **CIRCLE 638**

PC/104 MODULE FEATURES 16-MHZ CPU

Double the performance of current XT-architecture single-board computers can be attained from the CoreModule/XTPlus. The module, which fits the PC/104 form factor, features a 16-bit 16-MHz NEC V51 (8086 superset) microprocessor and up to 2 Mbytes of on-board RAM. It also contains two serial ports, one parallel port, a bootable solid-state disk, and a battery-backed real-time clock. The total power draw is 1.35 W at +5 V. In quantities of 100, the CoreModule/XTPlus sells for $356. A development kit is also available. RN

Ampro Computers Inc., 990 Almanor Ave., Sunnyvale, CA 94086; (408) 522-2100. **CIRCLE 639**

PWM CONTROLLER IC CORRECTS POWER FACTOR AND REGULATES VOLTAGE



Power-factor correction is becoming as important as line and load regulation for off-line switching power supplies. Until now, implementation of both has required two separate switching regulators—each with its own PWM controller and a number of redundant components. But in an industry first, Micro Linear has combined the two controllers in one 16-pin DIP. The ML4824 builds a power-factor corrected switch-mode power supply.

The IC combines the circuits required to implement a current or voltage mode boost-type power-factor correction (PFC) pulse-width modulator (PWM) and a synchronized current-mode PWM (for regulation). The latter PWM modulator is synchronized to run at exactly twice the switching frequency of the PFC modulator. The higher frequency (to 500 kHz) permits the use of smaller passive components.

The power-factor correction circuit employs a current-feed multiplier, so it can use either average current sensing or voltage-mode feed forward. The circuit achieves power factors on the order of 0.99, resulting in low-input conversion efficiencies of better than 95%. The ML4824 is aimed at power supplies designed to work off the rectified ac power lines world-side. The power-factor correction circuits contain an over-voltage comparator, which shuts down the PFC modulator in the event of a sudden decrease in load. The PFC circuits also provide peak current limiting and brown-out protection. They include a precision duty-cycle limit function, which prevents transformer saturation. In lots of 1000, the ML4824 goes for $3.80 each.

***Micro Linear Corp.**, 2092 Concourse Dr., San Jose, CA 95121; Gordon Cook, (408) 433-5200.* **CIRCLE 640**

■ *FRANK GOODENOUGH*

MOSFET-DRIVER IC SHRINKS POWER SUPPLIES

A 500-V dc, 2-A, half-bridge gate-driver IC includes an on-chip pulse-width-modulation oscillator to simplify the design, shrink the size, and increase the reliability of off-line power supplies and lighting controls. The HIP5500 half-bridge MOSFET driver's on-chip oscillator integrates all half-bridge control, logic, and gate-driver functions. It replaces a timer IC and glue logic while incorporating all the functionality of a full half-bridge controller/driver. The oscillator runs at either constant frequency and duty cycle or with a variable duty cycle set by an external voltage. In a 20-pin plastic DIP, the HIP5500 costs $4.16 in lots of 100. An SOIC version goes for $4.48. DM

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901; (800) 4-HARRIS, ext. 7206. **CIRCLE 641**

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A line of high-density motor-control modules is designed for three-phase applications. The OMS, OMD, and OMC series represent various circuit configurations. The OMS is a three-phase power switch, the OMD adds MOSFET gate drivers, and the OMC is a complete 30-A, three-phase motor controller. Ratings are from 15 to 45 A up to 600 V. Features include full closed-loop control of dc motors, full pulse-width-modulation circuitry, adjustable over-current protection, speed control down to zero RPM, shunt resistors, and linear thermal sensors. Devices can be tailored to specific needs. Pricing is from $195.56 in lots of 100 with delivery from stock to 12 weeks. DM

Omnirel Corp., 205 Crawford St., Leominster, MA 01453; (508) 534-5776. **CIRCLE 642**

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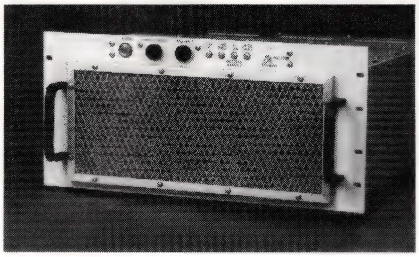
6-KVA DC-TO-AC INVERTER PUMPS OUT 7.5 KW

A precision fixed sinusoidal output with less than 2% total harmonic distortion is provided by the 6KVA ACE Series inverter. The rack-mountable unit, which is conservatively rated at 6 kVA, delivers 7500 W or up to 125 A of instantaneous peak current. That's more than many units rated at 8 kVA. This level of performance comes in a package that weighs in at less than 75 lbs. and fits in a 5U (8.75 in.) panel height.

The inverter's performance is achieved through high-frequency fabrication of the output waveform using pulse-width modulation, which replicates a reference sine wave with the appropriate amplitude scaling. Synthesizing the sine wave in this manner eliminates the need for large, bulky low-frequency filters and permits operation of the inverter into rectifier or non-linear loads with minimal voltage distortion.

Typical specifications include input-voltage ranges of 24, 48, 72, 120, and 270 V dc with an output voltage of 115 V ac rms, ±1%. The output frequency is 50, 60, or 400 Hz ±0.1%.



Ruggedness is built into the inverter. It's intended for mobile military and severe industrial environments and is designed to meet MIL-STD-810D shock and vibration requirements. It's also immune to humidity, fungus growth, and salt-fog corrosion.

One application for the unit is in a U.S. Army vehicle. The inverter, mounted in the Army's "Humvee" vehicle made famous in the Persian Gulf war, operates from the engine alternator and thus replaces a 350-lb. ac-generator set for powering radios and other equipment. The unit shown has built-in test features including a low input-voltage alarm, summary fault, and system-status indicators. A washable dust filters covers dual cooling fans. With its high inrush-current capability, the unit has many potential uses powering motors and non-linear, low-power-factor loads such as air conditioners and switch-mode power supplies.

Pricing for the 6KVE ACE Series inverter is around $2 per watt in quantities of 100. Delivery is in 120 days after receipt of order.

Transistor Devices Inc.*, 85 Horsehill Rd., Cedar Knolls, NJ 07927; Ron Zeman, (201) 267-1900.* **CIRCLE 643**

■ *DAVID MALINIAK*

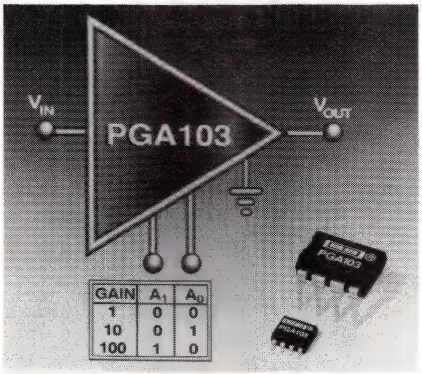
DESIGN-IN WASHABILITY

FREE Design Guide

When it comes to washable switches, NKK backs you with more sizes, more circuits and more quality than anyone else in the industry. NKK is your source for the first washable super-subminiature family, the smallest washable toggle, rocker and pushbutton devices, plus the world's most reliable switch contact mechanism (STC). So don't start your design without a free copy of our 456-page Design Guide and free tech support. Call 602/991-0942, FAX 602/998-1435 or write NKK Switches, 7850 E. Gelding Dr., Scottsdale, AZ 85260.

NKK® switches

GENERAL-PURPOSE PROGRAMMABLE-GAIN AMPLIFIER NOW AVAILABLE IN A 8-PIN DIP AND SOIC



The PGA103 is Burr-Brown's effort to do away with the image of the digitally controlled programmable-gain amplifier as an expensive, large, complex device. The new general-purpose device is available in 8-pin dual in-line packages as well as in small-outline ICs, and it provides gains of 1, 10, and 100 with a two-line address. Moreover, its price in quantities of 1000 is just $3.45.

Unlike most programmable-gain amplifiers, the PGA103's input is single ended, rather than differential. Consequently, the device should find its way into a large number of applications.

While it's not an ultra-precision device, the PGA103 has specifications that are sufficient for most general-purpose applications. Maximum gain nonlinearity (as a percent of full-scale range) at gains of 1, 10, and 100 run ±0.003, ±0.005, and ±0.02, respectively. Maximum gain error at gains of 1, 10, and 100 run ±0.02%, ±0.05%, and ±0.2%, respectively.

Gain vs. temperature at the three gains typically runs ±2, ±10, and ±30 ppm/°C. Maximum offset voltage (in µV referred to the input or RTI) at gains of 1, 10, and 100 run ±1500, ±500, and ±500. These typically change less than 5 µV/°C over the extended industrial temperature range.

The integrated circuit's –3 dB bandwidth, at the three fixed gains, typically runs 1.5, 0.75, and 0.25 MHz, while slew rate at all gains runs 9 V/µs. Settling time to 0.01% runs 2.5 µs at gains of 1 and 10; and 8 µs at a gain of 100. Voltage noise from 0.1 to 10 Hz runs less than 0.6 µVpk-pk.

The PGA103 operates from ±4.5 to ±18-V rails and needs just 3.5 mA of quiescent current.

***Burr-Brown Corporation**, Post Office Box 11400, Tucson, AZ 85734; contact Jason Albanus, (800) 548-6132.*

CIRCLE 644

■ *FRANK GOODENOUGH*

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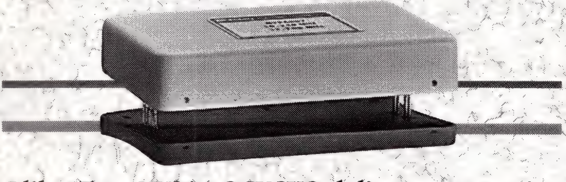
READER SERVICE 165

BLILEY CRYSTAL OSCILLATORS
For Digital Multiplex Systems!



Bliley Type NV9A OCVCXO delivers two precise timing signals, in fixed ratio, without PLL.
It's a new level of Stratum III performance.

CHECK THE SPECS	
Frequency Ratio:	3.2 constant (w/o PLL)
Frequencies (typical):	10.240 MHz and 32.768 MHz
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Frequency Deviation:	±10 x 10-6 min/0 to +10V
Power Supplies:	+15Vdc 30 mA max & +5Vdc 1.3A max
Size:	3.05" x 2.05" x 0.58" max

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READER SERVICE 162

Because you're thinking fast...

First we cut noise, distortion, settling time and power. Now...

Now we've made big cuts in prices too. Recent reductions in our op amp family averaged 25%, which means you get exceptional performance for your money. That applies to the newest additions to our low-noise, voltage-feedback op amp family too. For example:

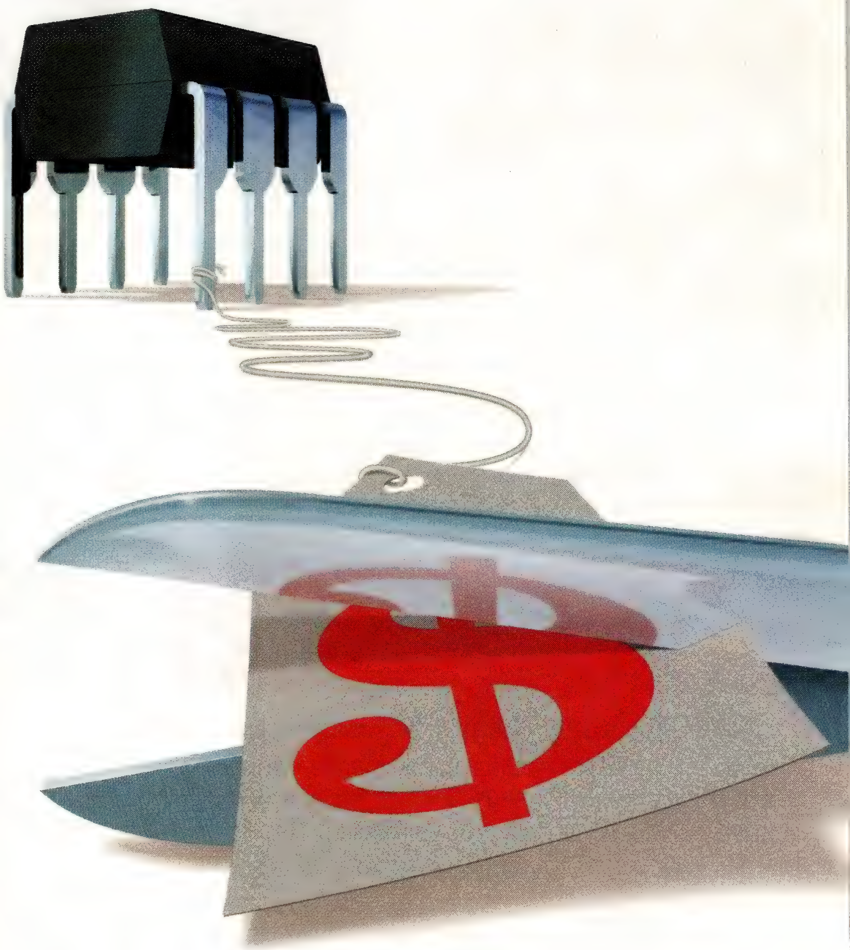
230MHz GBW, 1.6nV/$\sqrt{Hz}$ voltage noise, $3.95*.

Our new CLC426 couples high gain-bandwidth and low noise with a fast 400V/µs slew rate and 16ns settling time (0.05%). You get low distortion and adjustable supply current too. It's priced right for applications like wideband low-noise integrators, input buffers for hi-resolution A/Ds and other signal-conditioning applications requiring the combination of speed, low noise, low distortion and low dc errors.

Dual high-BW, low-noise op amp for $2.75/amp*.

In a class by itself, the new CLC428 packs two unity gain stable,135MHz GBW op amps with 2.0nV/$\sqrt{Hz}$ voltage noise in the same package. This leading-edge device also features a fast 400V/µs slew rate and 16ns settling time to 0.05%. This dual op amp offers great performance for the price and is ideal for multichannel integrator applications such as state-variable filters.

Don't cut yourself out of the best deals in op amps. Call today and find out just how much performance you can get for the money.



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Phone 44 203 422958, Fax 44 203 422961

*U.S. list price in 1,000s.

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READER SERVICE 186

DESIGN PLANNER PREDICTS CIRCUIT PERFORMANCE BEFORE LAYOUT

Timing-driven floorplanning, automatic partitioning, routability analysis, and base-array editing help Design Planner 2.2 predict circuit performance and area before routing and fabrication. The software addresses the physical design of both traditional and embedded submicron gate arrays.

Design Planner is a vendor-independent system that links synthesis tools from Synopsys and schematic capture from Viewlogic and Cadence to gate-array place-and-route tools from Cadence and Silvar-Lisco. Using its automatic interface, Design Planner reads timing estimates from synthesis, compares that data to calculations based on estimated or actual placement, and feeds back updated timing information via the Standard Delay Format interface.

The system's timing-driven floorplanning estimates and analyzes critical-path parasitics and delays. In fact, the floorplanner can accurately calculate propagation delays from Design Planner's detailed routing or placement estimates, using either capacitive or distributed resistance and capacitance information. Also, logic- and physical-partitioning algorithms within Design Planner automatically partition complex ASIC designs, and allow users to maximize their use of hierarchical design techniques for gate arrays. Users can analyze and display routing congestion, which helps reduce the number of times they must run a place-and-route tool.

Design Planner 2.2, which runs on Unix workstations, is available now. Pricing starts at $40,000 for node-locked licenses, and $52,000 for floating licenses.

High Level Design Systems Inc.,
2933 Bunker Hill Ln., No. 202,
Santa Clara, CA 95054; (408)
748-3456. **CIRCLE 645**

■ *LISA MALINIAK*

BOARD LAYOUT TOOLS RUN UNDER WINDOWS

WinBoard is a pc-board layout package that runs on a PC under MS Windows. It includes a new style of manual router that lets users create high-speed, analog, round, or dense boards. The program works through dialog boxes, which are used to set up parameters, save and load templates, and call for on-line help. View screens within the dialog boxes show users exactly what the target, pad stack, or mounting holes will look like before they are put on the board. On-line editing of track styles is one of many advancements that speed the layout process. Users can select a trace or arc of any angle without exiting the route mode. In addition, the backtracking feature immediately undoes a track segment or an entire track without exiting the route mode. WinBoard is shipping now for $995. LM

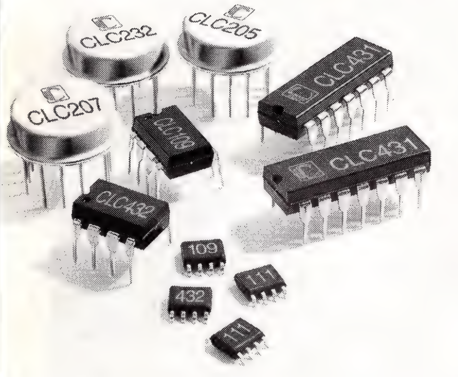
Ivex Design International, 15232 N.W. Greenbrier Pkwy., Beaverton, OR 97006; (503) 531-3555. **CIRCLE 646**

GRAPHICALLY DEBUG VERILOG DESCRIPTIONS

Version 2.0 of the Magellan debugging environment includes the new RTL-Spreadsheet viewer that lets users create block diagrams of their circuit, and then see the simulation output within these diagrams. That way, users can observe changing values that show the flow of data through the circuits as they debug their designs. Magellan is a graphical debugging environment for Verilog hardware-description-language simulators. It includes a Verilog graphic encapsulator, a waveform display, a 2D navigator, a source viewer, and the RTL-Spreadsheet viewer. Magellan is used with interactive Verilog, or with VCD files. Version 2.0, which runs on Hewlett-Packard, Silicon Graphics, or Sun Unix-based workstations, is available now. Pricing for the product begins at $1995. LM

Systems Science Inc., 1860 Embarcadero Rd., Suite 260, Palo Alto, CA 94303; (415) 812-1800. **CIRCLE 647**

Bargain buffers and wideband op amps.



Fast buffers use little power. Pick from two new closed-loop, unity-gain buffers for video switch buffers, testpoint drivers and very high-speed active filters. The 270MHz CLC109 delivers a 350V/µs slew rate at just 3.5mA (± 5V). And just for $1.49*. The 800MHz CLC111 slews at a blazing 3500V/µs at 10.5mA. And it's only $2.75*.

READER SERVICE 187

Dual op amps also combine speed, low power. For dual selectable-gain amplifiers, video signal multiplexing and a host of amplifier and driver applications, pick the 62MHz CLC431(with disable input) or the CLC432. They take 7mA/Amp, slew at 2000V/µs, support video specs and operate on ±5 to ±15V supplies. Priced at just $2.99* and $2.49* respectively.

READER SERVICE 190

Prices cut on ultra-high-performance hybrids. Need great distortion specs for fast, precision ADs and receiver IF stages? How about high output swing? Check the prices on our 170 MHz, high-gain CLC205 and CLC207. And the low gain, 270MHz CLC232. All three combine high speed with ultra low distortion. And prices start at just $24.50*.

*U.S. list price in 1,000s.

READER SERVICE 191

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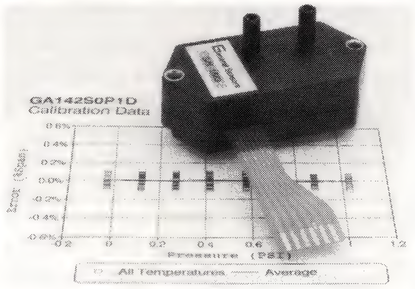
PRESSURE SENSORS ELIMINATE ADC

A family of smart, fully digital pressure sensors for precision instrumentation eliminates the need for an external a-d converter because communication is achieved by means of a TTL-compatible, synchronous, serial digital interface. The GA142S (standard), GA142F (fast), and GA142HR (high-resolution) sensors also feature a single 5-V supply, low power consumption, and traceability by serial number. Each series offers several standard pressure ranges from 1 to 100 psi full scale in both differential and absolute configurations. The GA142F is claimed to be the first of its kind to satisfy the 8-ms response time required by medical instrumentation. Typical linearity is 0.01%. OEM pricing is under $80 for the standard line and under $100 for the fast and high-resolution types. Delivery is in from 2 to 4 weeks. DM

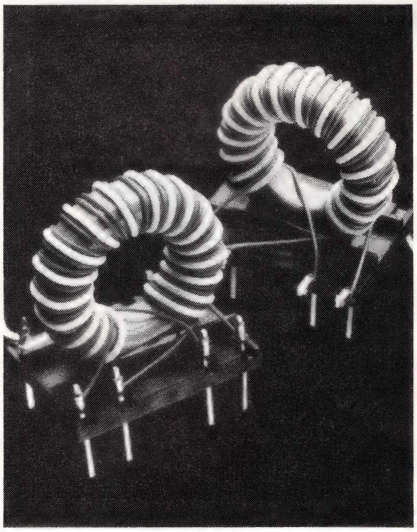


General Sensors, 1249 Reamwood Ave., Sunnyvale, CA 94089; Timothy Shotter, (408) 734-1851.

CIRCLE 648

TRANSFORMERS OFFER FAST RISE TIMES

The lowest interwinding capacitance and leakage inductance in the industry is claimed for the GDT Series of FET gate-drive transformers. As a result, the transformers offer extremely fast rise times for switching frequencies of more than 100 kHz. The devices are designed with three insulating barriers from primary to secondary and 4200-V rms hi-pot withstanding capability. Two fully floating outputs are provided, each having a 1-to-1 turns ratio with respect to the input. Three models are optimized for use at operating frequencies of 25, 50, or 100 kHz. Pricing in OEM quantities starts at $1.82. Delivery is from stock. DM



GFS Manufacturing Inc., 140 Crosby Rd., Dover, NH 03820-4371; (603) 742-4375. **CIRCLE 649**

The Best Points About
CHO-SEAL® 3000 EMI Gaskets...

Are Their Low Points

- Low Cost - less than half the price of traditional conductive elastomers.
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- Low Effort Installation - without adhesives.

They have their high points, too. Like shielding effectiveness of over 70 dB from 30 MHz to 1GHz, and a wide range of standard cross sections.

Find out why Chomerics® CHO-SEAL 3000 EMI shielding gaskets are scoring high points in hundreds of commercial electronic products.

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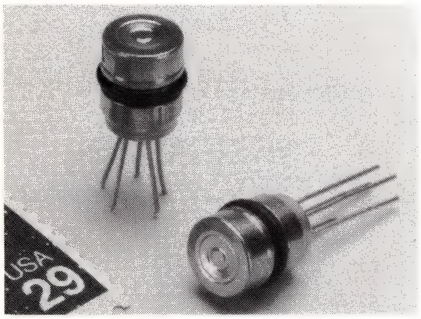
The National Arbor Day Foundation

PRESSURE SENSOR WORKS IN ALL MEDIA

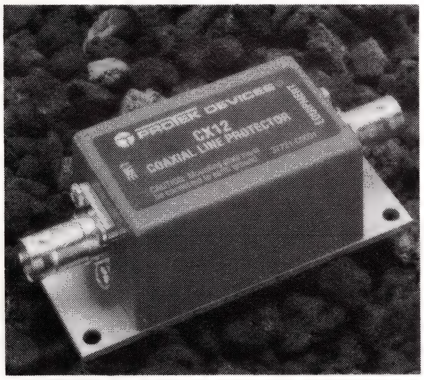
A combination of advanced packaging technology and the company's silicon micromachined pressure-sensing element has resulted in the NPI-21A Series of ultra-miniature, all-media sensors. The device is designed for easy integration into systems measuring gas or liquid pressures. A rugged, 316L stainless-steel welded package contains sensors for either zero-to-3000-psi or zero-to-5000-psi ranges with non-linearity of less than 0.1% full-scale output (FSO) typical. Full-scale unamplified output is 240 mV typical with output-signal thermal accuracy of ±1% FSO typical over the range of –10 to 85°C. Pricing is $25.50 in lots of 1000. Delivery is in 4 to 6 weeks. DM



Lucas NovaSensor, 1055 Mission Ct., Fremont, CA 94539; (510) 490-9100. **CIRCLE 650**

TRANSIENT PROTECTOR GUARDS COAX LINES

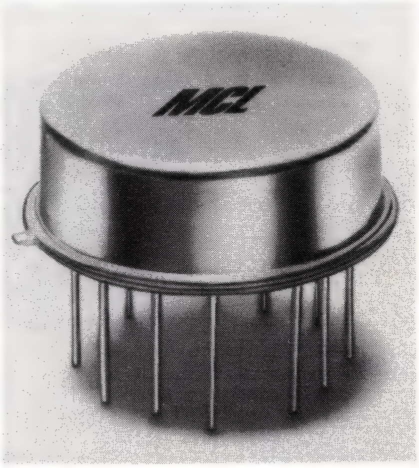
With the CX12 coaxial-line protectors, interfacing equipment is protected from transients caused by lightning, inductive switching, and electrostatic discharge. The devices are particularly suited for safeguarding audio-visual, video, Ethernet, token-ring, and other LAN-interface systems requiring coaxial cables. The two-stage hybrid devices provide primary and secondary levels of protection. Two models are offered. The standard CX12 is designed for speeds of less than 10 MHz and has an operating data-rate range up to 10 Mbytes. The CX12LC is for speeds above 10 MHz and handles data rates up to 100 Mbytes. In lots of 100, unit pricing for either device is $69. Delivery is from stock to 4 weeks. DM



ProTek Devices, P.O. Box 3129, Tempe, AZ 85280-3129; David Hutchins, (602) 968-6060. **CIRCLE 651**

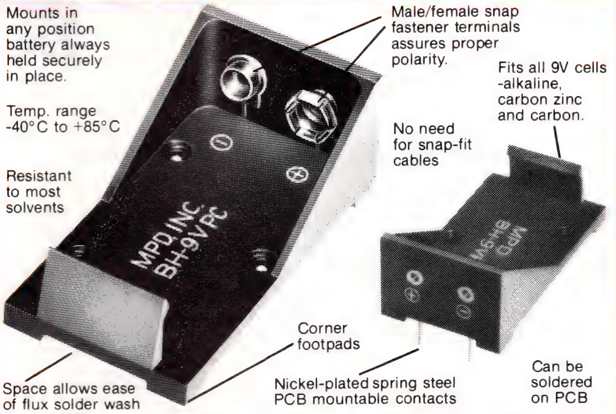
THREE-WAY SPLITTER DIVIDES POWER

Combining cost effectiveness and performance, the TO8SC-3-1W three-way 50-Ω power splitter offers extremely wide-band coverage from 80 to 800 MHz. The splitter provides high typical isolation of 25 dB and low mid-band insertion loss of 0.5 dB. Other features include excellent amplitude balance of 0.15 dB typical and phase balance of 1.0 typical. Maximum input power is 1 W and internal power dissipation is 0.375 W maximum. Housed in a hermetically sealed TO-8 can with a 0.6-in. diameter, the unit's operating-temperature range is –55 to 100°C. Pricing is $29.95 each. DM



Mini-Circuits, P.O. Box 350166, Brooklyn, NY 11235-0003; (718) 934-4500. **CIRCLE 652**

PCB MOUNTABLE
9V BATTERY HOLDER
BH9V-PC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Fits all 9V cells -alkaline, carbon zinc and carbon.
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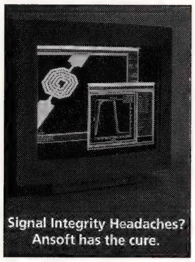
READER SERVICE 181

CATALOG/LITERATURE REVIEW

Signal Integrity & EMI/EMC

Maxwell SI Eminence offers a unique, integrated solution to the whole spectrum of high speed design issues from signal delays to EMI/EMC. Characterize effects to analyze complex electronic designs.

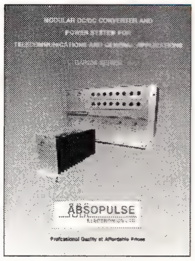


CIRCLE 215

Ansoft Corporation

Battery Chargers

The PFC Rectifier delivers 500W to load or Battery (2500W per rack), Features include full electronic protection, redundancy, high MTBF and hot swapping. The series is available in rack mount or stand-alone format.



CIRCLE 216

Absopulse Electronics

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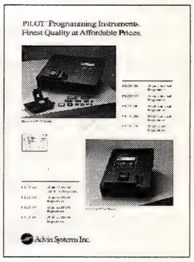
Affordable, dependable & versatile, Advin offers a full line of device programmers. All pkg types supported. IC mfrs approved. Free lifetime s/w updates via electronic BBS. Call for free catalog & latest supported devices list.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Use DACI's Handbook to achieve reliable, cost effective, optimized designs, without the need for complex math.

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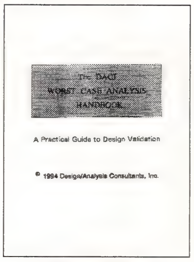
Analyzer software.

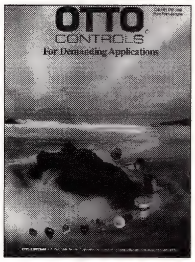

The DACI
WORST CASE ANALYSIS
HANDBOOK
A Practical Guide to Design Validation
© 1994 Design/Analysis Consultants, Inc.

CIRCLE 218

Design Analysis Consultants, Inc.

Snap-Action Switches

All new Catalog 105 has 72 pages featuring the new sealed rocker K Series and detailing an in-depth line of precision snap-action pushbutton, toggle, rocker, limit and basic switches. All feature OTTO's unique design assuring low contact resistance, high contact pressure and long cycle life. Quality made in the U.S.A.

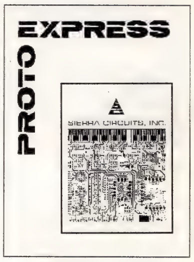


CIRCLE 219

OTTO CONTROLS

PROTO EXPRESS

Multilayer prototypes in 1 to 5 days. FR4 and polyimide. Commerical or Milspect capabilities *buried/blind VIAS* carbon paste* up to 22 layers. Call Ken or Joycie 408-735-7137 phone 408-735-1408.



CIRCLE 220

Proto Express

Highspeed Waveform Capture

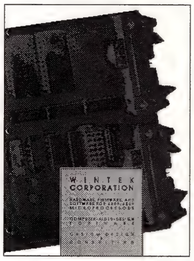
Signatec, Corona, CA. - A binder containing data sheets for all of its pc based products for use in the areas of waveform capture, waveform generation and signal processing can be obtained by contacting them at (909) 734-3001

CIRCLE 221

Signatec Inc.

Microcomputer Modules & CAD

The catalog describes 6800 and 6809 single-board computers, input/output interfaces debuggers, compilers and assemblers; plus schematic capture and printed circuit board layout software and accessories for the IBM personal computer.

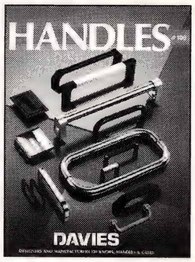


CIRCLE 222

Wintek Corporation

Davies Molding Catalog

Features Attractive Top of The Line Handles Davies Molding Company, Carol Stream, Illinois is introducing an attractive and comprehensive new 56 page Handle catalog. Catalog #100 introduces unique top of the line Handles for machine tool, medical, electrical and transportation equipment applications. For a copy of Catalog #100 use the circle number to the right.



CIRCLE 223

DAVIES MOLDING CO.

VLSI/SMT SOLUTIONS CATALOG

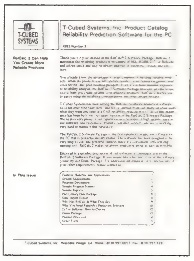
Free '94 catalog. Over 3500 devices; 120 "off-the-shelf" items available for overnight delivery. Unlimited application consulting. Ask about our custom designs. Leading edge technology --over 500 PQFP Solutions. Time Saving Solutions.

CIRCLE 224

EMULATION TECHNOLOGY

Reliability Prediction

Catalog describes the RelCalc2 software Package, which automates Mil-HDBK-217 or Bellcore on your PC, and allows quick and easy reliability analysis of your electronic products. Phone: (818) 991-0057 Fax: (818) 991-1281

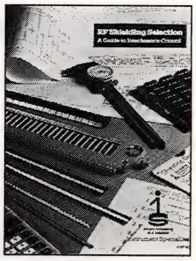

T-Cubed Systems, Inc. Product Catalog
Reliability Prediction Software for the PC

CIRCLE 225

T-Cubed Systems

SHIELDING CATALOG

28-Pg Publication details instrument specialties BECU shielding and grounding products. Also included is information on metals compatibility, testing, engineering kits, platinting engineered stampings and assemblies and ordering.

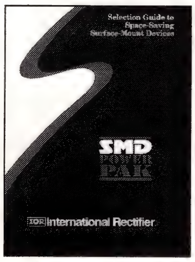


CIRCLE 226

INSTRUMENT SPECIALTIES

Power SMDs Selection Guide

Some 250 space-saving surface mount devices covering both N and P channel power MOSFETS, Schottky diodes, IGBTs, and MOS Gate Drivers are all featured in this SMD Product Selection Guide from International Rectifier, El Sequndo, CA.

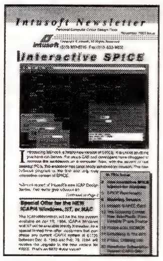


CIRCLE 227

INTERNATIONAL RECTIFIER

Spice Application Notes

The Intusoft Newsletter is a FREE publication that discusses the SPICE circuit simulation program. It contains technical articles on simulation and modeling, as well as an introduction to the NEW Interactive version of IsSpice.



CIRCLE 228

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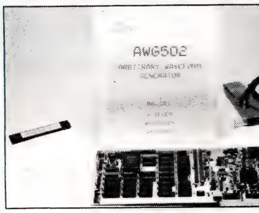

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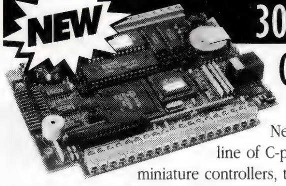

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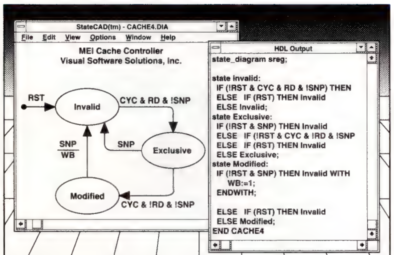

```
state_diagram sreg;

state Invalid:
  IF (!RST & CYC & RD & !SNP) THEN
  ELSE   IF (RST) THEN Invalid
  ELSE Invalid;
state Exclusive:
  IF (!RST & SNP) THEN Invalid
  ELSE   IF (!RST & CYC & !RD & !SNP
  ELSE   IF (RST) THEN Invalid
  ELSE Exclusive;
state Modified:
  IF (!RST & SNP) THEN Invalid WITH
      WB:=1;
  ENDWITH;

  ELSE   IF (RST) THEN Invalid
  ELSE Modified;
END CACHE4
```

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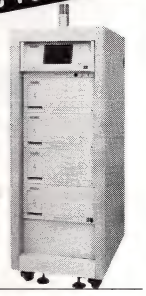

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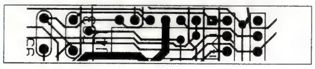

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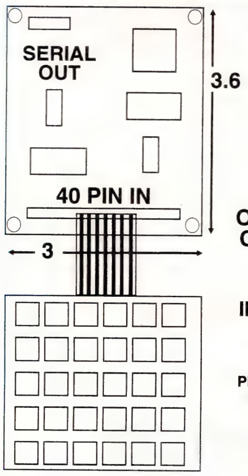

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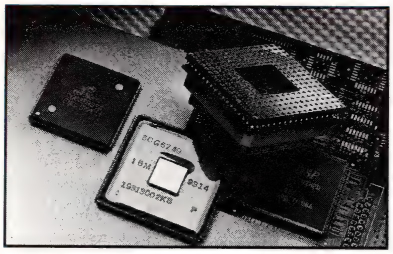

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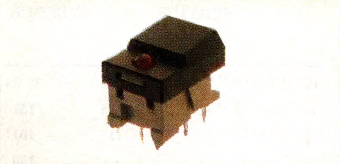

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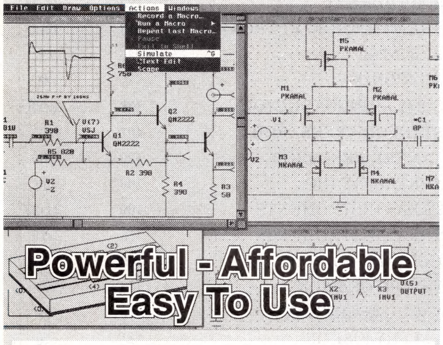

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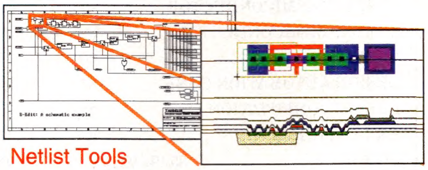

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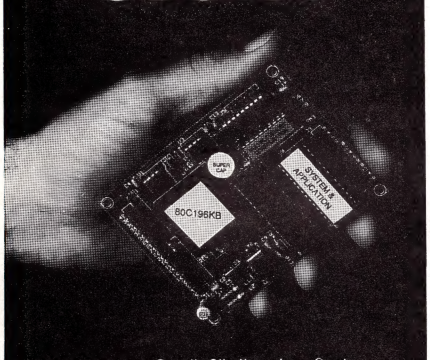

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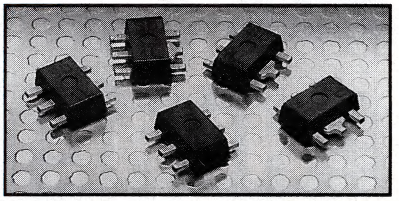

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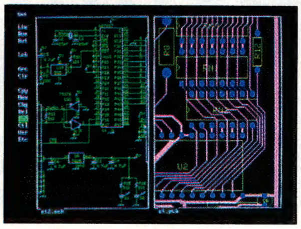

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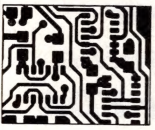

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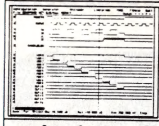

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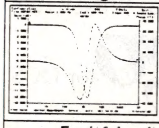

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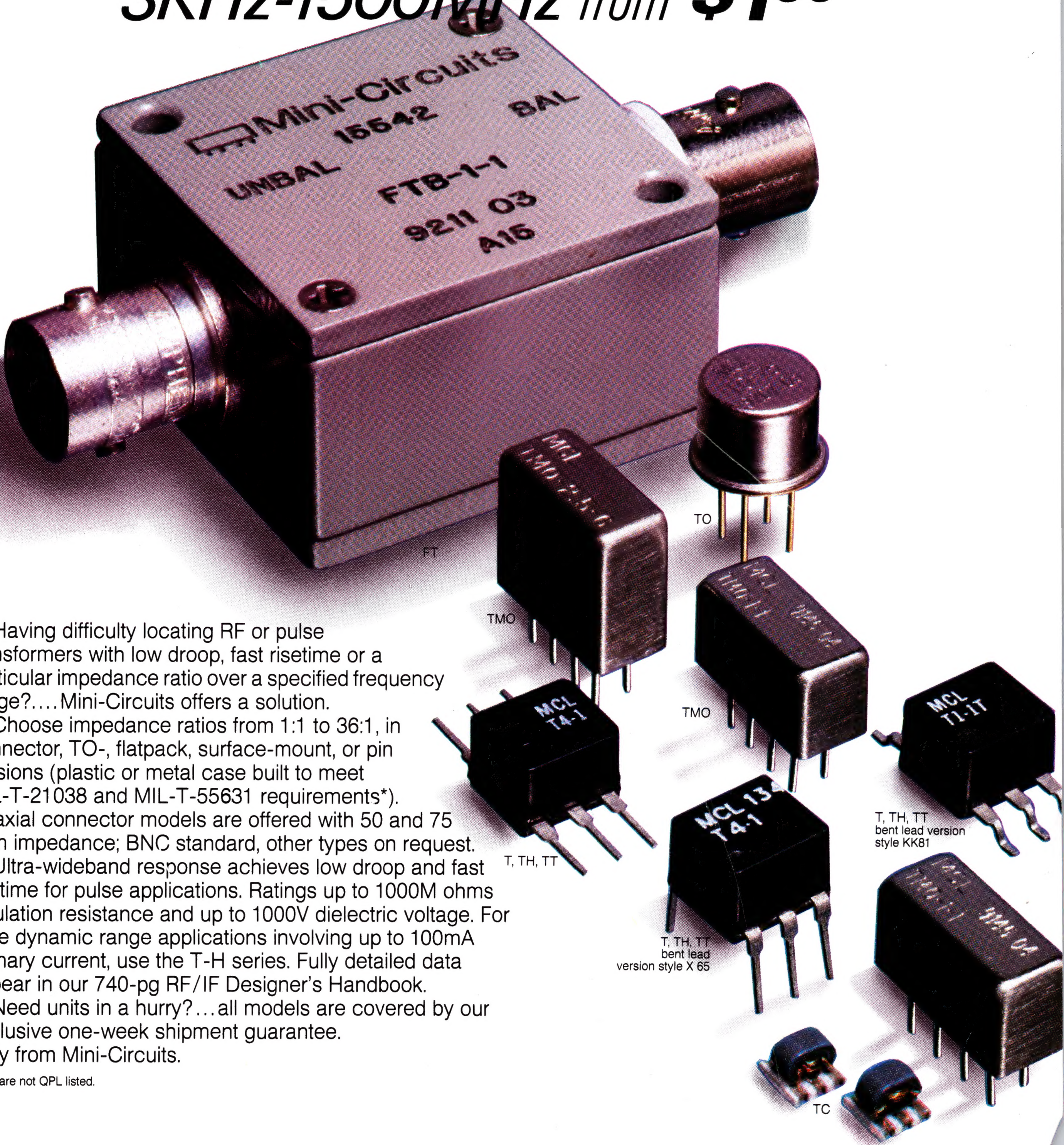

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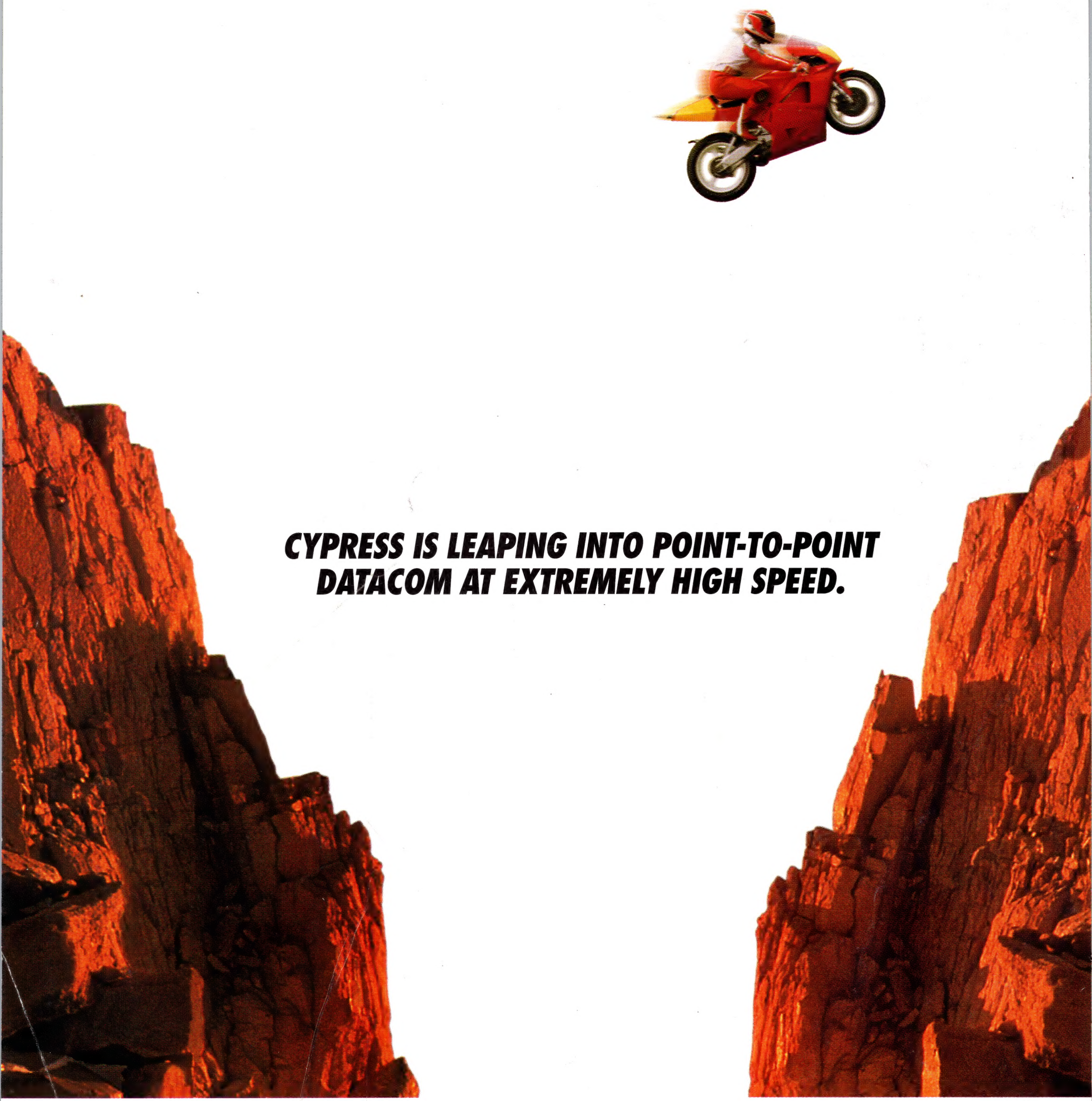
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